- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **PNP Inputs Reduce DC Loading**
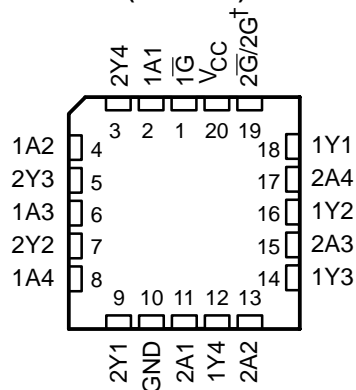- **Hysteresis at Inputs Improves Noise Margins**

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical, active-low output-control ($\overline{G}$) inputs, and complementary output-control (G and $\overline{G}$) inputs. These devices feature high fan-out, improved fan-in, and 400-mV noise margin. The SN74LS' and SN74S' devices can be used to drive terminated lines down to 133 Ω.

SN54LS', SN54S' . . . J OR W PACKAGE
SN74LS240, SN74LS244 . . . DB, DW, N, OR NS PACKAGE
SN74LS241 . . . DW, N, OR NS PACKAGE
SN74S' . . . DW OR N PACKAGE
(TOP VIEW)

1$\overline{G}$	1		20	V$_{CC}$
1A1	2		19	2$\overline{G}$/2G†
2Y4	3		18	1Y1
1A2	4		17	2A4
2Y3	5		16	1Y2
1A3	6		15	2A3
2Y2	7		14	1Y3
1A4	8		13	2A2
2Y1	9		12	1Y4
GND	10		11	2A1
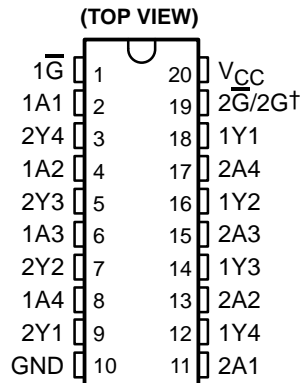
† 2G for 'LS241 and 'S241 or 2$\overline{G}$ for all other drivers.

SN54LS', SN54S' . . . FK PACKAGE
(TOP VIEW)

Pins (top, left to right): 2Y4, 1A1, 1$\overline{G}$, V$_{CC}$, 2$\overline{G}$/2G†
Pin numbers top: 3, 2, 1, 20, 19

1A2	4	18	1Y1
2Y3	5	17	2A4
1A3	6	16	1Y2
2Y2	7	15	2A3
1A4	8	14	1Y3

Pin numbers bottom: 9, 10, 11, 12, 13
Pins (bottom): 2Y1, GND, 2A1, 1Y4, 2A2

† 2G for 'LS241 and 'S241 or 2$\overline{G}$ for all other drivers.

TEXAS INSTRUMENTS

schematics of inputs and outputs

'LS240, 'LS241, 'LS244

'S240, 'S241, 'S244

EQUIVALENT OF EACH INPUT

V_CC

9 kΩ NOM

Input

EQUIVALENT OF EACH INPUT

V_CC

Req

Input

G and $\overline{\text{G}}$ inputs: R_{eq} = 2 kΩ NOM
A inputs: R_{eq} = 2.8 kΩ NOM

TYPICAL OF ALL OUTPUTS

V_CC

R

Output

GND

'LS240. 'LS241, 'LS244: R = 50 Ω NOM
'S240, 'S241, S244: R = 25 Ω NOM

TEXAS
INSTRUMENTS

logic diagram
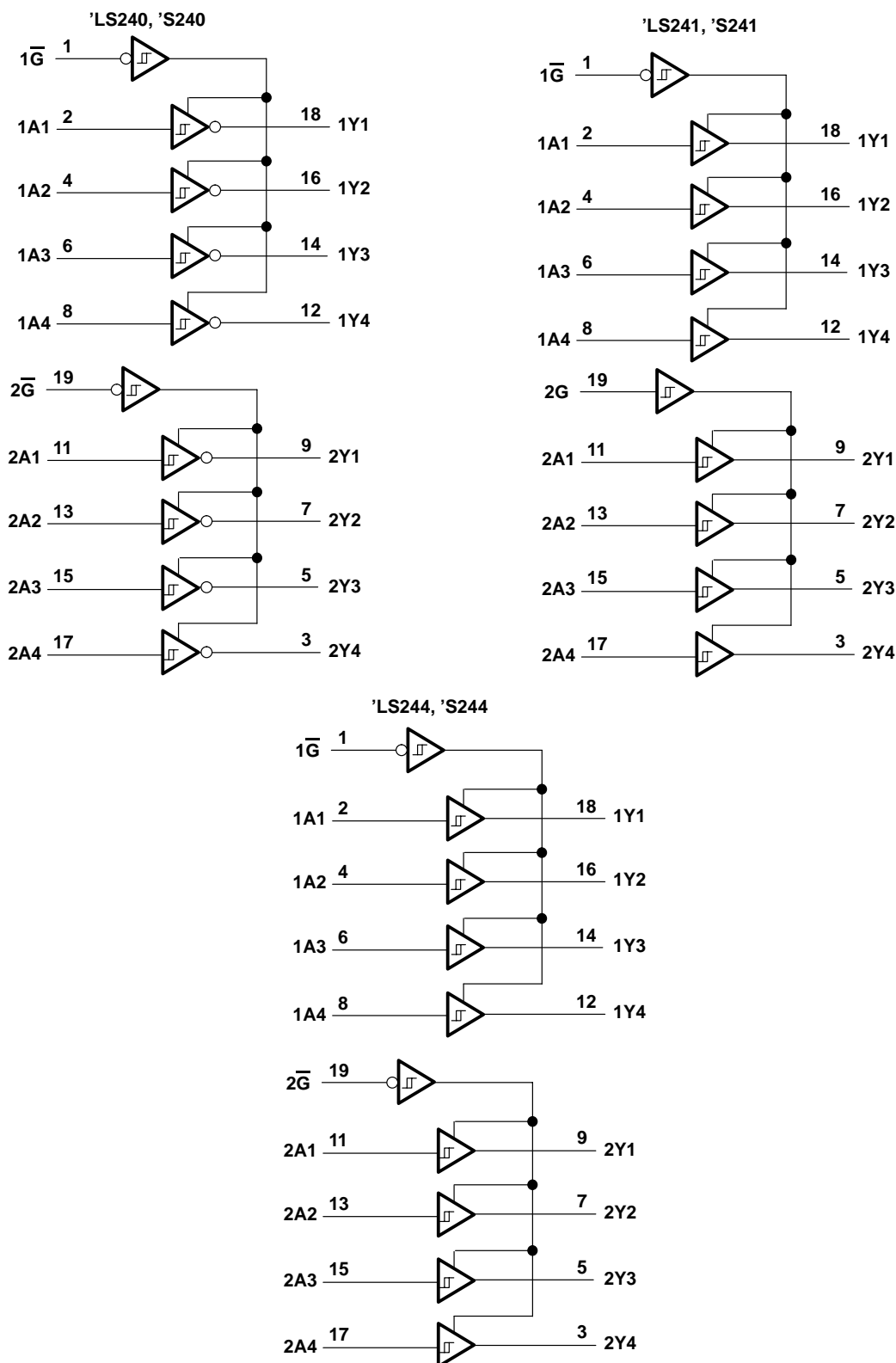
Pin numbers shown are for DB, DW, J, N, NS, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) .... 7 V
Input voltage, V_I: 'LS .... 7 V
               'S .... 5.5 V
Off-state output voltage .... 5.5 V
Package thermal impedance, θ_{JA} (see Note 2): DB package .... 70°C/W
                                      DW package .... 58°C/W
                                      N package .... 69°C/W
                                      NS package .... 60°C/W
Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.
           2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			–12			–15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

TEXAS INSTRUMENTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			SN54LS'			SN74LS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
Hysteresis $(V_{T+} - V_{T-})$	V_{CC} = MIN			0.2	0.4		0.2	0.4		V
V_{OH}	V_{CC} = MIN, I_{OH} = −3 mA	V_{IH} = 2 V,	V_{IL} = MAX,	2.4	3.4		2.4	3.4		V
	V_{CC} = MIN, I_{OH} = MAX	V_{IH} = 2 V,	V_{IL} = 0.5 V,	2			2			
V_{OL}	V_{CC} = MIN, V_{IL} = MAX	V_{IH} = 2 V,	I_{OL} = 12 mA			0.4			0.4	V
			I_{OL} = 24 mA						0.5	
I_{OZH}	V_{CC} = MAX, V_{IL} = MAX	V_{IH} = 2 V,	V_O = 2.7 V			20			20	µA
I_{OZL}	V_{CC} = MAX, V_{IL} = MAX	V_{IH} = 2 V,	V_O = 0.4 V			−20			−20	µA
I_I	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V				20			20	µA
I_{IL}	V_{CC} = MAX,	V_{IL} = 0.4 V				−0.2			−0.2	mA
I_{OS}§	V_{CC} = MAX,			−40		−225	−40		−225	mA
I_{CC}	V_{CC} = MAX, Output open	Outputs high	All		17	27		17	27	mA
		Outputs low	'LS240		26	44		26	44	
			'LS241, 'LS244		27	46		27	46	
		Outputs disabled	'LS240		29	50		29	50	
			'LS241, 'LS244		32	54		32	54	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER	TEST CONDITIONS		'LS240			'LS241, 'LS244			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	R_L = 667 Ω,	C_L = 45 pF		9	14		12	18	ns
t_{PHL}				12	18		12	18	
t_{PZL}	R_L = 667 Ω,	C_L = 45 pF		20	30		20	30	ns
t_{PZH}				15	23		15	23	
t_{PLZ}	R_L = 667 Ω,	C_L = 5 pF		10	20		10	20	ns
t_{PHZ}				15	25		15	25	

recommended operating conditions

		SN54S' MIN	SN54S' NOM	SN54S' MAX	SN74S' MIN	SN74S' NOM	SN74S' MAX	UNIT
V_{CC}	Supply voltage (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
	External resistance between any input and V_{CC} or ground			40			40	kΩ
T_A	Operating free-air temperature (see Note 3)	−55		125	0		70	°C

NOTES: 1. Voltage values are with respect to network ground terminal.
 3. An SN54S241J operating at free-air temperature above 116°C requires a heat sink that provides a thermal resistance from case to free air, $R_{\theta CA}$, of not more that 40°C/W.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			SN54S' MIN	SN54S' TYP‡	SN54S' MAX	SN74S' MIN	SN74S' TYP‡	SN74S' MAX	UNIT
V_{IK}	V_{CC} = MIN,	I_I = −18 mA				−1.2			−1.2	V
Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = MIN			0.2	0.4		0.2	0.4		V
V_{OH}	V_{CC} = MIN I_{OH} = −1 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,					2.7		V
	V_{CC} = MIN, I_{OH} = −3 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,	2.4	3.4		2.4	3.4		
	V_{CC} = MIN, I_{OH} = MAX	V_{IH} = 2 V,	V_{IL} = 0.5 V,	2			2			
V_{OL}	V_{CC} = MIN, I_{OL} = MAX	V_{IH} = 2 V,	V_{IL} = 0.8 V,			0.55			0.55	V
I_{OZH}	V_{CC} = MAX, V_{IL} = 0.8 V	V_{IH} = 2 V,	V_O = 2.4 V			50			50	µA
I_{OZL}	V_{CC} = MAX, V_{IL} = 0.8 V	V_{IH} = 2 V,	V_O = 0.5 V			−50			−50	µA
I_I	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V				50			50	µA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V	Any A			−400			−400	µA
			Any G			−2			−2	mA
I_{OS}§	V_{CC} = MAX			−50		−225	−50		−225	mA
I_{CC}	V_{CC} = MAX, Output open	Outputs high	'S240		80	123		80	135	mA
			'S241,'S244		95	147		95	160	
		Outputs low	'S240		100	145		100	150	
			'S241, 'S244		120	170		120	180	
		Outputs disabled	'S240		100	145		100	150	
			'S241, 'S244		120	170		120	180	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244
SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SDLS144B – APRIL 1985 – REVISED FEBRUARY 2002

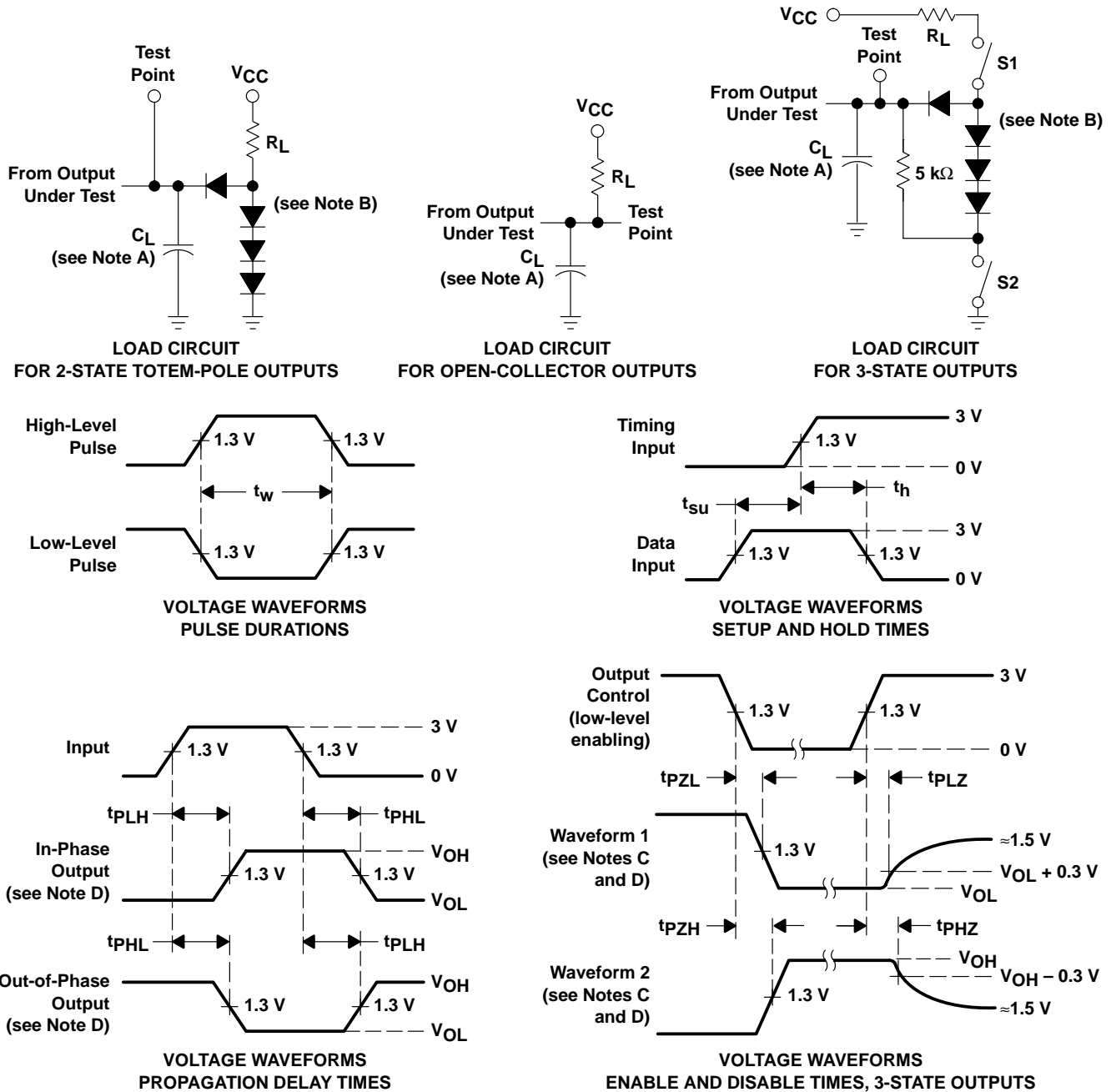**switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 2)**

PARAMETER	TEST CONDITIONS		'S240			'S241, 'S244			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	R_L = 90 Ω,	C_L = 50 pF		4.5	7		6	9	ns
t_{PHL}				4.5	7		6	9	
t_{PZL}	R_L = 90 Ω,	C_L = 50 pF		10	15		10	15	ns
t_{PZH}				6.5	10		8	12	
t_{PLZ}	R_L = 90 Ω,	C_L = 5 pF		10	15		10	15	ns
t_{PHZ}				6	9		6	9	

TEXAS
INSTRUMENTS

SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244
SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS
SDLS144B – APRIL 1985 – REVISED FEBRUARY 2002

PARAMETER MEASUREMENT INFORMATION
SERIES 54LS/74LS DEVICES

LOAD CIRCUIT
FOR 2-STATE TOTEM-POLE OUTPUTS

LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS

LOAD CIRCUIT
FOR 3-STATE OUTPUTS

VOLTAGE WAVEFORMS
PULSE DURATIONS

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
  B. All diodes are 1N3064 or equivalent.
  C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
     Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.
  E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
  F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O ≈ 50 Ω, t_r ≤ 15 ns, t_f ≤ 6 ns.
  G. The outputs are measured one at a time with one input transition per measurement.

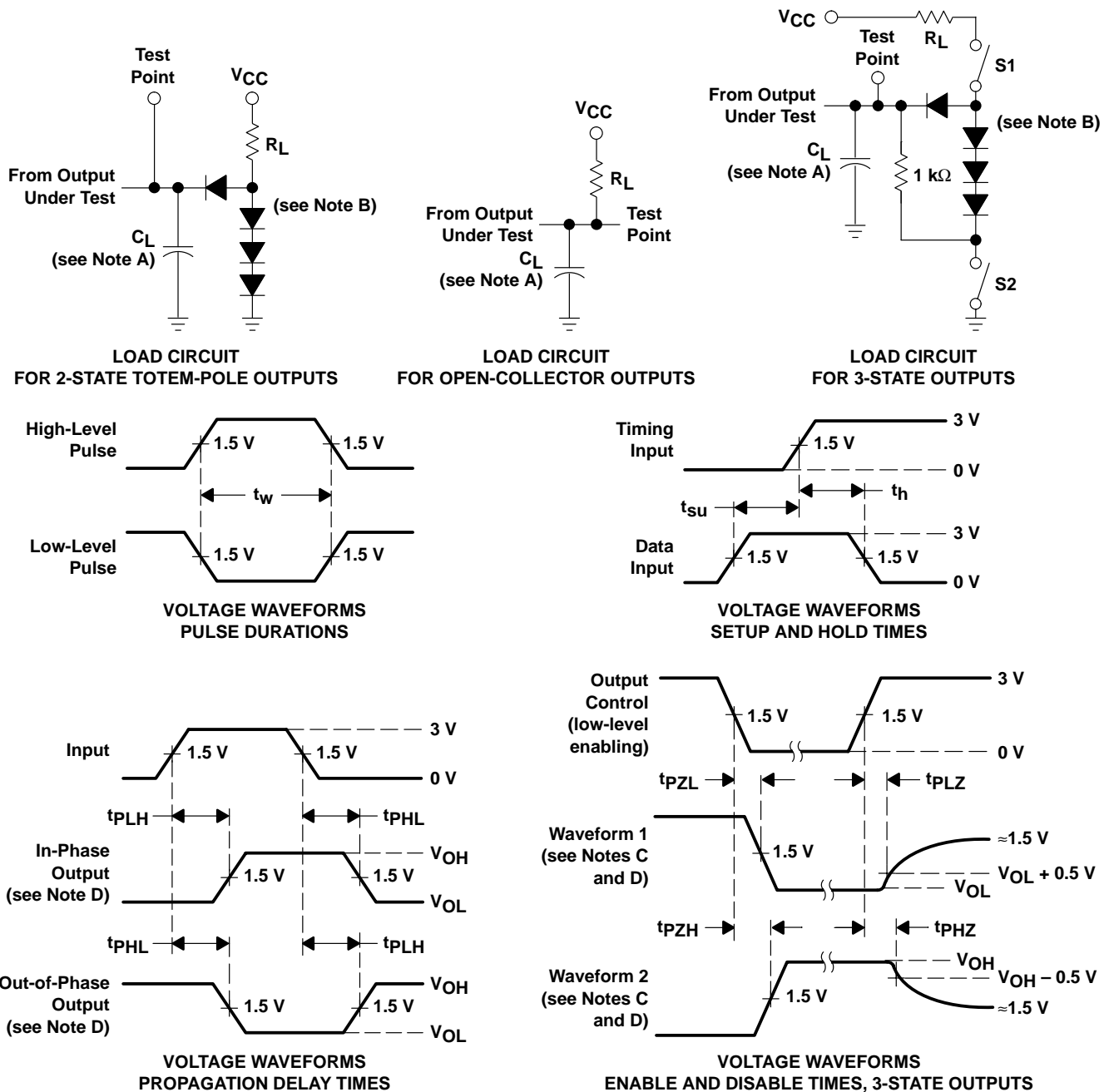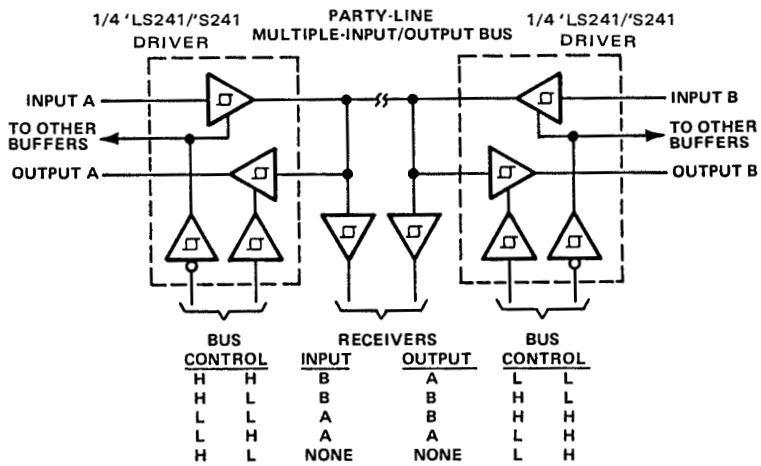**Figure 1. Load Circuits and Voltage Waveforms**

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PARAMETER MEASUREMENT INFORMATION
SERIES 54S/74S DEVICES

**LOAD CIRCUIT
FOR 2-STATE TOTEM-POLE OUTPUTS**

**LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS**

**LOAD CIRCUIT
FOR 3-STATE OUTPUTS**

**VOLTAGE WAVEFORMS
PULSE DURATIONS**

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**

**VOLTAGE WAVEFORMS
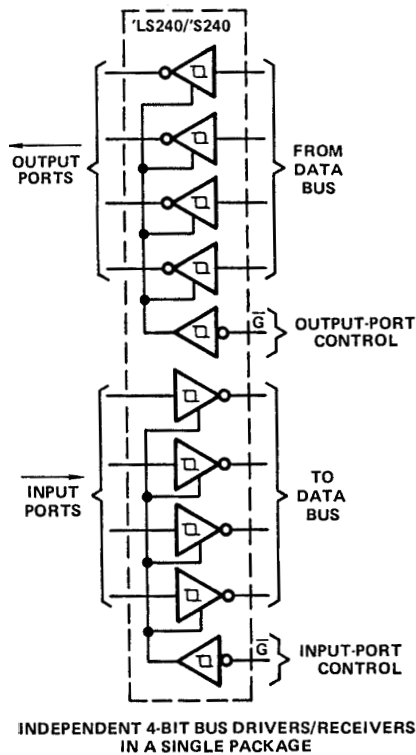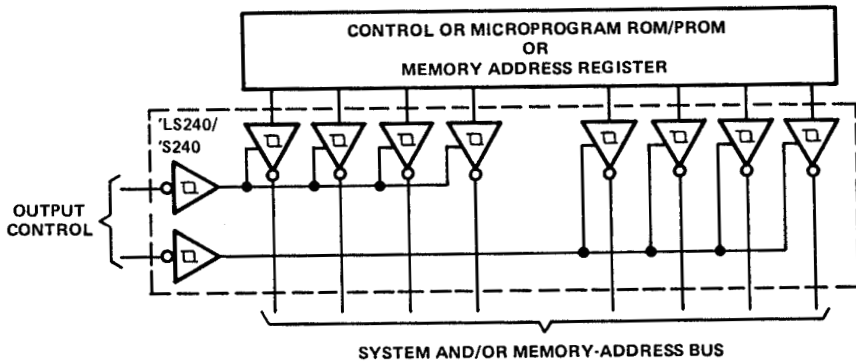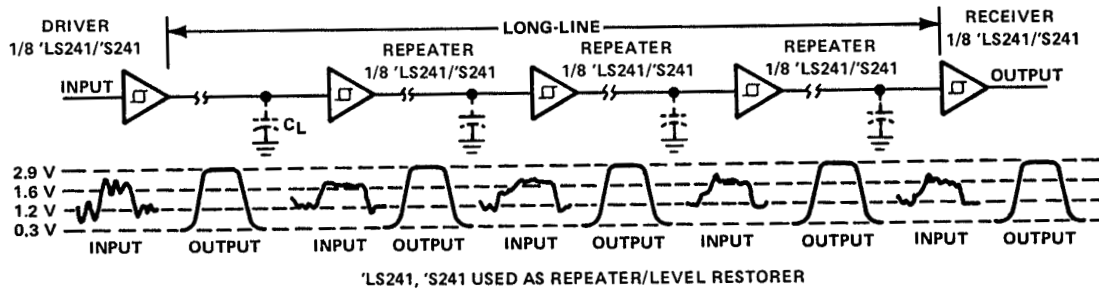ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS**

NOTES: A. C_L includes probe and jig capacitance.
   B. All diodes are 1N3064 or equivalent.
   C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
       Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.
   E. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 1 MHz, $Z_O \approx$ 50 Ω; t_r and $t_f \leq$ 7 ns for Series
       54/74 devices and t_r and $t_f \leq$ 2.5 ns for Series 54S/74S devices.
   F. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

APPLICATION INFORMATION

'LS241, 'S241 USED AS REPEATER/LEVEL RESTORER

'LS240/'S240 USED AS SYSTEM AND/OR MEMORY BUS DRIVER—4-BIT
ORGANIZATION CAN BE APPLIED TO HANDLE BINARY OR BCD

INDEPENDENT 4-BIT BUS DRIVERS/RECEIVERS
IN A SINGLE PACKAGE

BUS CONTROL		RECEIVERS INPUT	OUTPUT	BUS CONTROL	
H	H	B	A	L	L
H	L	B	B	H	L
L	L	A	B	H	H
L	H	A	A	L	H
H	L	NONE	NONE	L	H

PARTY-LINE BUS SYSTEM
WITH MULTIPLE INPUTS, OUTPUTS, AND RECEIVERS