![TEXAS INSTRUMENTS]

CD54HC139, CD74HC139, CD54HCT139, CD74HCT139

High-Speed CMOS Logic
Dual 2- to 4-Line Decoder/Demultiplexer

September 1997 - Revised October 2003

Features

- **Multifunction Capability**
  - **Binary to 1 of 4 Decoders or 1 to 4 Line Demultiplexer**

- **Active Low Mutually Exclusive Outputs**

- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . 15 LSTTL Loads**

- **Wide Operating Temperature Range . . . -55°C to 125°C**

- **Balanced Propagation Delay and Transition Times**

- **Significant Power Reduction Compared to LSTTL Logic ICs**

- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**

- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL} = 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

- **Memory Decoding, Data Routing, Code Conversion**

Description

The 'HC139 and 'HCT139 devices contain two independent binary to one of four decoders each with a single active low enable input ($\overline{1E}$ or $\overline{2E}$). Data on the select inputs (1A0 and 1A1 or 2A0 and 2A1) cause one of the four normally high outputs to go low.

If the enable input is high all four outputs remain high. For demultiplexer operation the enable input is the data input. The enable input also functions as a chip select when these devices are cascaded. This device is functionally the same as the CD4556B and is pin compatible with it.

The outputs of these devices can drive 10 low power Schottky TTL equivalent loads. The HCT logic family is functionally as well as pin equivalent to the LS logic family.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE
CD54HC139F3A	-55 to 125	16 Ld CERDIP
CD54HCT139F3A	-55 to 125	16 Ld CERDIP
CD74HC139E	-55 to 125	16 Ld PDIP
CD74HC139M	-55 to 125	16 Ld SOIC
CD74HC139MT	-55 to 125	16 Ld SOIC
CD74HC139M96	-55 to 125	16 Ld SOIC
CD74HCT139E	-55 to 125	16 Ld PDIP
CD74HCT139M	-55 to 125	16 Ld SOIC
CD74HCT139MT	-55 to 125	16 Ld SOIC
CD74HCT139M96	-55 to 125	16 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

Pinout

**CD54HC139, CD54HCT139
(CERDIP)
CD74HC139, CD74HCT139
(PDIP, SOIC)
TOP VIEW**

$\overline{1E}$	1		16	V_{CC}
1A0	2		15	$\overline{2E}$
1A1	3		14	2A0
$\overline{1Y0}$	4		13	2A1
$\overline{1Y1}$	5		12	$\overline{2Y0}$
$\overline{1Y2}$	6		11	$\overline{2Y1}$
$\overline{1Y3}$	7		10	$\overline{2Y2}$
GND	8		9	$\overline{2Y3}$

1

Functional Diagram
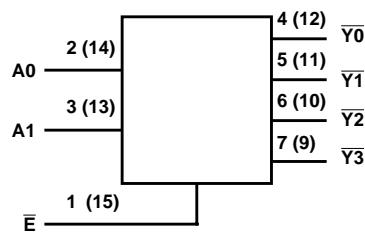
TRUTH TABLE

INPUTS ENABLE SELECT			OUTPUTS			
$\overline{E}$	A1	A0	$\overline{Y3}$	$\overline{Y2}$	$\overline{Y1}$	$\overline{Y0}$
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1
1	X	X	1	1	1	1

X = Don't Care, Logic 1 = High, Logic 0 = Low

Logic Diagram

2
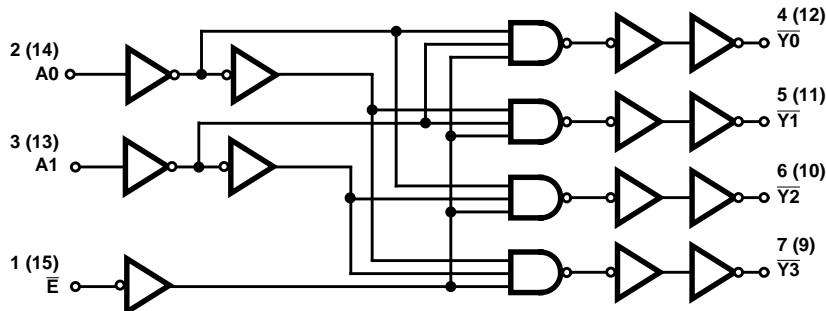
CD54HC139, CD74HC139, CD54HCT139, CD74HCT139

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
  For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . ±20mA
DC Output Diode Current, I_{OK}
  For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . ±20mA
DC Output Source or Sink Current per Output Pin, I_O
  For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} or I_{GND} . . . . ±50mA

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
E (PDIP) Package	67
M (SOIC) Package.	73

Maximum Junction Temperature . . . . 150°C
Maximum Storage Temperature Range . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C
  (SOIC - Lead Tips Only)

Operating Conditions

Temperature Range (T_A) . . . . -55°C to 125°C
Supply Voltage Range, V_{CC}
  HC Types . . . . .2V to 6V
  HCT Types . . . . .4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . 0V to V_{CC}
Input Rise and Fall Time
  2V . . . . 1000ns (Max)
  4.5V. . . . . 500ns (Max)
  6V . . . . 400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	µA

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
HCT TYPES												
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} and GND	0	5.5	-		±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	5.5	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC} (Note 2)	V_{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTE:

2. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
All	0.7

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g., 360µA max at 25°C.

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
HC TYPES											
Propagation Delay	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	145	-	180	-	220	ns
A0, A1 to Outputs			4.5	-	-	29	-	36	-	44	ns
			6	-	-	25	-	31	-	38	ns
$\overline{E}$ to Outputs	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	135	-	170	-	205	ns
			4.5	-	-	27	-	34	-	41	ns
			6	-	-	23	-	29	-	35	ns
Select to Output	t_{PLH}, t_{PHL}	C_L = 15pF	5	-	12	-	-	-	-	-	ns
Enable to Output	t_{PLH}, t_{PHL}	C_L = 15pF	5	-	11	-	-	-	-	-	ns

Switching Specifications Input t_r, t_f = 6ns **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Output Transition Time (Figure 1)	t_{TLH}, t_{THL}	C_L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Power Dissipation Capacitance, (Notes 3, 4)	C_{PD}	-	5	-	55	-	-	-	-	-	pF
Input Capacitance	C_{IN}	-	-	-	-	10	-	10	-	10	pF
HCT TYPES											
Propagation Delay											
A0, A1 to Outputs	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	34	-	43	-	51	ns
$\overline{E}$ to Outputs	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	34	-	43	-	51	ns
Select to Output	t_{PLH}, t_{PHL}	C_L = 15pF	5	-	14	-	-	-	-	-	ns
Enable to Output	t_{PLH}, t_{PHL}	C_L = 15pF	5	-	14	-	-	-	-	-	ns
Output Transition Time (Figure 2)	t_{TLH}, t_{THL}	C_L = 50pF	4.5	-	-	15	-	19	-	22	ns
Power Dissipation Capacitance, (Notes 3, 4)	C_{PD}	-	5	-	59	-	-	-	-	-	pF
Input Capacitance	C_{IN}	-	-	-	-	10	-	10	-	10	pF

NOTES:

3. C_{PD} is used to determine the dynamic power consumption, per decoder/demux.

4. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where: f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

## *Test Circuits and Waveforms*
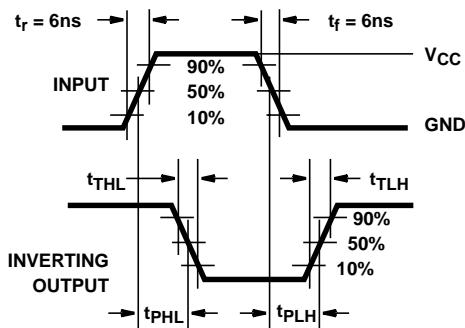
**FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGA-TION DELAY TIMES, COMBINATION LOGIC**
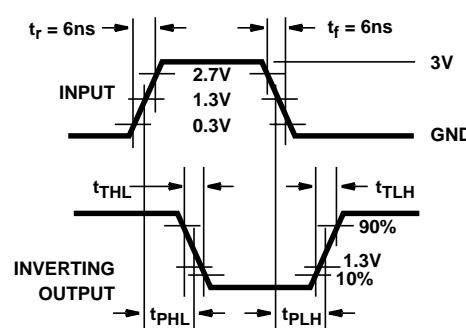
FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC