TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS145D

CD54HC132, CD74HC132, CD54HCT132, CD74HCT132

High-Speed CMOS Logic Quad 2-Input NAND Schmitt Trigger

August 1997 - Revised August 2003

Features

- **Unlimited Input Rise and Fall Times**
- **Exceptionally High Noise Immunity**
- **Typical Propagation Delay: 10ns at V_{CC} = 5V, C_L = 15pF, T_A = 25^oC**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55^oC to 125^oC**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 37%, N_{IH} = 51% of V_{CC} at V_{CC} = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

Description

The ’HC132 and ’HCT132 each contain four 2-input NAND Schmitt Triggers in one package. This logic device utilizes silicon gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The HCT logic family is functionally pin compatible with the standard LS logic family.

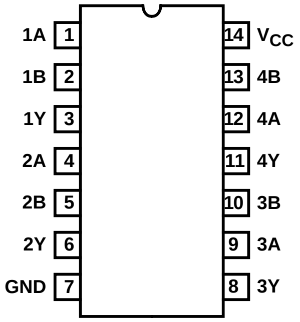
Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE
CD54HC132F3A	-55 to 125	14 Ld CERDIP
CD54HCT132F3A	-55 to 125	14 Ld CERDIP
CD74HC132E	-55 to 125	14 Ld PDIP
CD74HC132M	-55 to 125	14 Ld SOIC
CD74HC132MT	-55 to 125	14 Ld SOIC
CD74HC132M96	-55 to 125	14 Ld SOIC
CD74HCT132E	-55 to 125	14 Ld PDIP
CD74HCT132M	-55 to 125	14 Ld SOIC
CD74HCT132MT	-55 to 125	14 Ld SOIC
CD74HCT132M96	-55 to 125	14 Ld SOIC

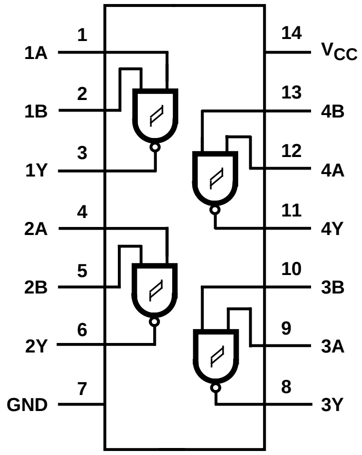
NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

Pinout

CD54HC132, CD54HCT132
(CERDIP)
CD74HC132, CD74HCT132
(PDIP, SOIC)
TOP VIEW



Functional Diagram

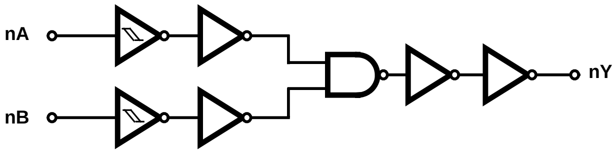


TRUTH TABLE

INPUTS		OUTPUT
nA	**nB**	**nY**
L	L	H
L	H	H
H	L	H
H	H	L

H = High Voltage Level, L = Low Voltage Level

Logic Symbol



Absolute Maximum Ratings

DC Supply Voltage, V_{CC}	-0.5V to 7V
DC Input Diode Current, I_{IK}	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	±20mA
DC Output Diode Current, I_{OK}	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	±20mA
DC Output Source or Sink Current per Output Pin, I_O	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	±25mA
DC V_{CC} or Ground Current, I_{CC} or I_{GND}	±50mA

Operating Conditions

Temperature Range (T_A)	-55°C to 125°C
Supply Voltage Range, V_{CC}	
HC Types	2V to 6V
HCT Types	4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O	0V to V_{CC}
Input Rise and Fall Time	
2V	100ms (Max)
4.5V	100ms (Max)
6V	100ms (Max)

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
E (PDIP) Package	80
M (SOIC) Package	86
Maximum Junction Temperature	150°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) (SOIC - Lead Tips Only)	300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
Input Switch Points (Note 2)	V_T+	-	-	2	0.7	-	1.5	0.7	1.5	0.7	1.5	V
				4.5	1.7	-	3.15	1.7	3.15	1.7	3.15	V
				6	2.1	-	4.2	2.1	4.2	2.1	4.2	V
	V_T-	-	-	2	0.3	-	1	0.3	1	0.3	1	V
				4.5	0.9	-	2.2	0.9	2.2	0.9	2.2	V
				6	1.2	-	3	1.2	3	1.2	3	V
	V_H			2	0.2	-	1	0.2	1	0.2	1	V
				4.5	0.4	-	1.4	0.4	1.4	0.4	1.4	V
				6	0.6	-	1.6	0.6	1.6	0.6	1.6	V
High Level Output Voltage CMOS Loads	V_{OH}	V_T+ or V_T-	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V

DC Electrical Specifications (Continued)

		TEST CONDITIONS			25°C			-40°C TO 85°C		-55°C TO 125°C		
PARAMETER	**SYMBOL**	**V_I (V)**	**I_O (mA)**	**V_{CC} (V)**	**MIN**	**TYP**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
Low Level Output Voltage CMOS Loads	V_{OL}	V_T+ or V_T-	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	2	-	20	-	40	µA
HCT TYPES												
Input Switch Points (Note 2)	V_T+	-	-	4.5	1.2	-	1.9	1.2	1.9	1.2	1.9	V
				5.5	1.4	-	2.1	1.4	2.1	1.4	2.1	V
	V_T-	-	-	4.5	0.5	-	1.2	0.5	1.2	0.5	1.2	V
				5.5	0.6	-	1.4	0.6	1.4	0.6	1.4	V
	V_H	-	-	4.5	0.4	-	1.4	0.4	1.4	0.4	1.4	V
				5.5	0.4	-	1.5	0.4	1.5	0.4	1.5	V
High Level Output Voltage CMOS Loads	-	V_T+ or V_T-	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_T+ or V_T-	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} and GND	-	5.5	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	5.5	-	-	2	-	20	-	40	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC} (Note 3)	V_{CC} - 2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTES:

2. Hysteresis definition, characteristic and test setup see Test Circuits and Waveforms
3. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
nA, nB	0.6

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g. 360μA max at 25°C.

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay A, B to Y (Figure 1)	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	125	-	156	-	188	ns
			4.5	-	-	25	-	31	-	38	ns
			6	-	-	21	-	27	-	32	ns
Propagation Delay A, B to Y	t_{TLH}, t_{THL}	C_L = 15pF	5	-	10	-	-	-	-	-	pF
Transition Times (Figure 1)	t_{TLH}, t_{THL}	C_L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C_I	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 4, 5)	C_{PD}	-	5	-	30	-	-	-	-	-	pF
HCT TYPES											
Propagation Delay A, B to Y (Figure 2)	t_{PHL}, t_{PHL}	C_L = 50pF	4.5	-	-	33	-	41	-	50	ns
Propagation Delay A, B to Y	t_{PLH}, t_{PHL}	C_L = 15pF	5	-	13	-	-	-	-	-	pF
Transition Times (Figure 2)	t_{TLH}, t_{THL}	C_L = 50pF	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	C_I	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 4, 5)	C_{PD}	-	5	-	30	-	-	-	-	-	pF

NOTES:

4. C_{PD} is used to determine the dynamic power consumption, per gate.
5. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

Test Circuits and Waveforms

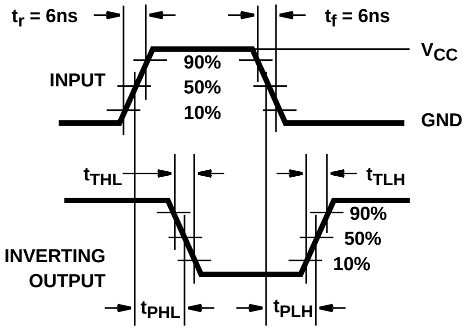


FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

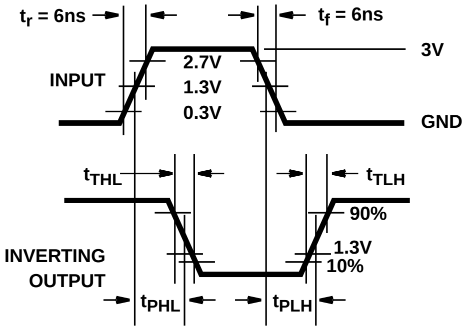


FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

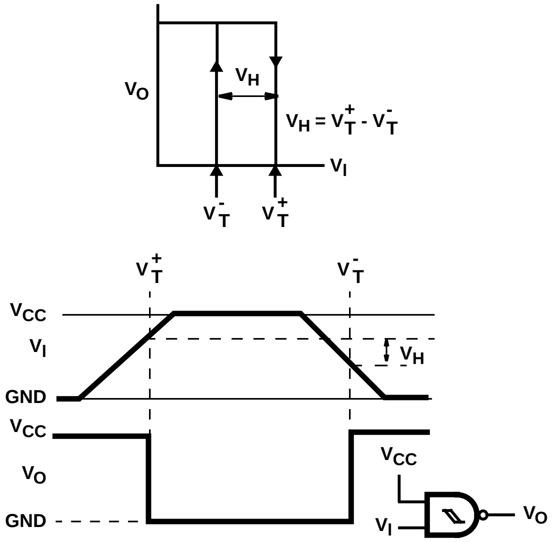


FIGURE 3. HYSTERESIS DEFINITION, CHARACTERISTIC, AND TEST SET-UP