

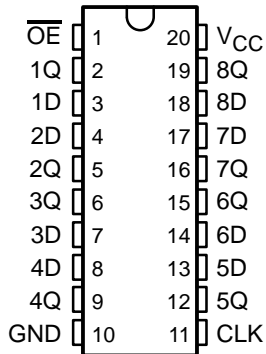
# SN54AHCT374, SN74AHCT374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS241L – OCTOBER 1995 – REVISED JULY 2003

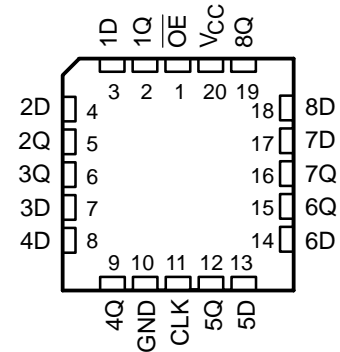
- Inputs Are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per JESD 17

- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

SN54AHCT374 . . . J OR W PACKAGE  
SN74AHCT374 . . . DB, DGV, DW, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54AHCT374 . . . FK PACKAGE  
(TOP VIEW)



## description/ordering information

The 'AHCT374 devices are octal edge-triggered D-type flip-flops that feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels of the data (D) inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74AHCT374N	SN74AHCT374N
	SOIC – DW	Tube	SN74AHCT374DW	AHCT374
		Tape and reel	SN74AHCT374DWR	
	SOP – NS	Tape and reel	SN74AHCT374NSR	AHCT374
	SSOP – DB	Tape and reel	SN74AHCT374DBR	HB374
	TSSOP – PW	Tube	SN74AHCT374PW	HB374
Tape and reel		SN74AHCT374PWR		
	TVSOP – DGV	Tape and reel	SN74AHCT374DGVR	HB374
–55°C to 125°C	CDIP – J	Tube	SNJ54AHCT374J	SNJ54AHCT374J
	CFP – W	Tube	SNJ54AHCT374W	SNJ54AHCT374W
	LCCC – FK	Tube	SNJ54AHCT374FK	SNJ54AHCT374FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2003, Texas Instruments Incorporated  
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# SN54AHCT374, SN74AHCT374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS241L – OCTOBER 1995 – REVISED JULY 2003

## description/ordering information (continued)

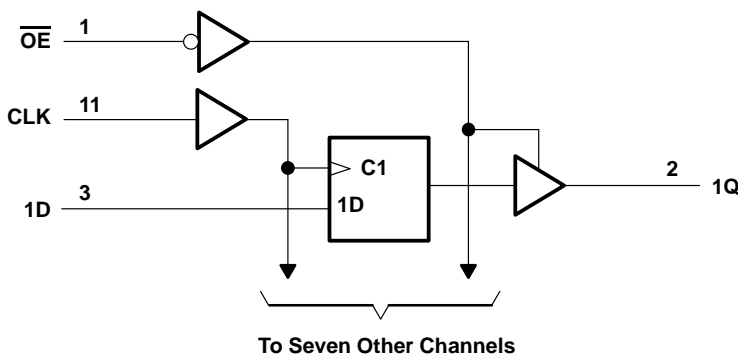
$\overline{OE}$  does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE  
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	$Q_0$
H	X	X	Z

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	-0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
DB package	70°C/W
DGV package	92°C/W
DW package	58°C/W
N package	69°C/W
NS package	60°C/W
PW package	83°C/W
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# SN54AHCT374, SN74AHCT374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS241L – OCTOBER 1995 – REVISED JULY 2003

## recommended operating conditions (see Note 3)

		SN54AHCT374		SN74AHCT374		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		-8		-8	mA
I <sub>OL</sub>	Low-level output current		8		8	mA
Δt/Δv	Input transition rise or fall rate		20		20	ns/V
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AHCT374		SN74AHCT374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	4.5 V	4.4	4.5		4.4		4.4	V	
	I <sub>OH</sub> = -8 mA		3.94			3.8		3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V			0.1			0.1	V	
	I <sub>OL</sub> = 8 mA				0.36		0.44	0.44		
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V			±0.1		±1*	±1	μA	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND, V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	5.5 V			±0.25		±2.5	±2.5	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		40	40	μA	
ΔI <sub>CC</sub> †	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			1.35		1.5	1.5	mA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4	10			10	pF	
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V		9					pF	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

† This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

## timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T <sub>A</sub> = 25°C		SN54AHCT374		SN74AHCT374		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, CLK high or low	6.5		6.5		6.5		ns
t <sub>su</sub>	Setup time, data before CLK↑	2.5		2.5		2.5		ns
t <sub>h</sub>	Hold time, data after CLK↑	2.5		2.5		2.5		ns

# SN54AHCT374, SN74AHCT374

## OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

### WITH 3-STATE OUTPUTS

SCLS241L – OCTOBER 1995 – REVISED JULY 2003

switching characteristics over recommended free-air temperature operating range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHCT374		SN74AHCT374		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			$C_L = 15\text{ pF}$	90**	140**		80**		80		MHz
			$C_L = 50\text{ pF}$	85	130		75		75		
$t_{\text{PLH}}$	CLK	Q	$C_L = 15\text{ pF}$		5.6**	9.4**	1**	10.5**	1	10.5	ns
$t_{\text{PHL}}$					5.6**	9.4**	1**	10.5**	1	10.5	
$t_{\text{PZH}}$	$\overline{\text{OE}}$	Q	$C_L = 15\text{ pF}$		6.5**	10.2**	1**	11.5**	1	11.5	ns
$t_{\text{PZL}}$					6.5**	10.2**	1**	11.5**	1	11.5	
$t_{\text{PHZ}}$	$\overline{\text{OE}}$	Q	$C_L = 15\text{ pF}$		6.2**	10.2**	1**	11**	1	11	ns
$t_{\text{PLZ}}$					6.2**	10.2**	1**	11**	1	11	
$t_{\text{PLH}}$	CLK	Q	$C_L = 50\text{ pF}$		6.4	10.4	1	11.5	1	11.5	ns
$t_{\text{PHL}}$					6.4	10.4	1	11.5	1	11.5	
$t_{\text{PZH}}$	$\overline{\text{OE}}$	Q	$C_L = 50\text{ pF}$		7.3	11.2	1	12.5	1	12.5	ns
$t_{\text{PZL}}$					7.3	11.2	1	12.5	1	12.5	
$t_{\text{PHZ}}$	$\overline{\text{OE}}$	Q	$C_L = 50\text{ pF}$		7	11.2	1	12	1	12	ns
$t_{\text{PLZ}}$					7	11.2	1	12	1	12	
$t_{\text{sk(o)}}$			$C_L = 50\text{ pF}$			1***			1	ns	

\*\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

\*\*\* On products compliant to MIL-PRF-38535, this parameter does not apply.

noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 4)

PARAMETER		SN74AHCT374			UNIT
		MIN	TYP	MAX	
$V_{\text{OL(P)}}$	Quiet output, maximum dynamic $V_{\text{OL}}$		0.8	1.2	V
$V_{\text{OL(V)}}$	Quiet output, minimum dynamic $V_{\text{OL}}$		-0.8	-1.2	V
$V_{\text{OH(V)}}$	Quiet output, minimum dynamic $V_{\text{OH}}$	3.8			V
$V_{\text{IH(D)}}$	High-level dynamic input voltage	2			V
$V_{\text{IL(D)}}$	Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are for surface-mount packages only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

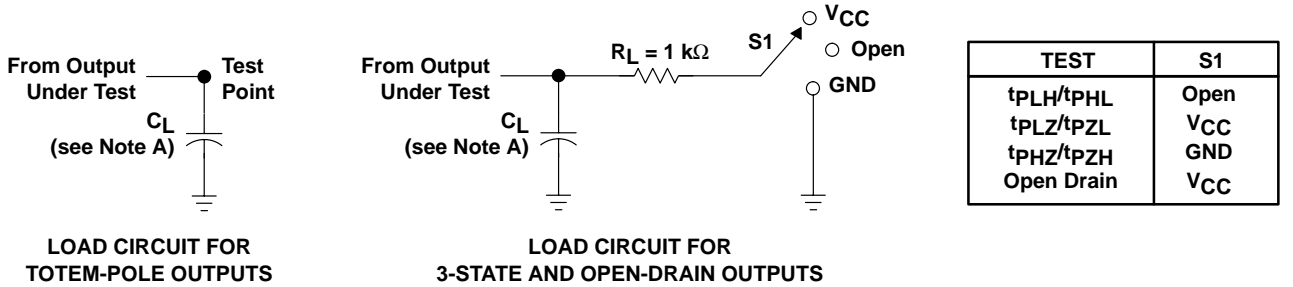
PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{\text{pd}}$	Power dissipation capacitance	No load, $f = 1\text{ MHz}$	27	pF



# SN54AHCT374, SN74AHCT374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

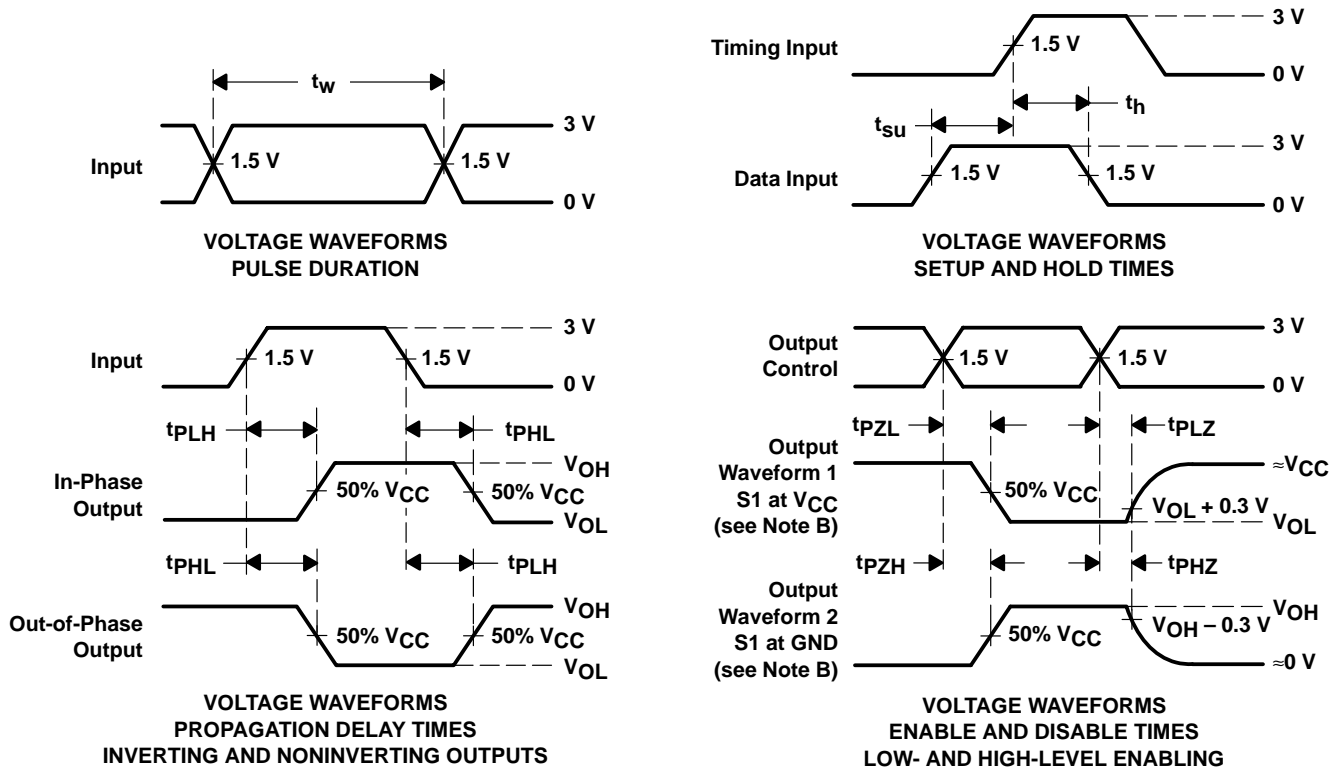
SCLS241L – OCTOBER 1995 – REVISED JULY 2003

## PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR  
TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR  
3-STATE AND OPEN-DRAIN OUTPUTS



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.
  - The outputs are measured one at a time with one input transition per measurement.
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms