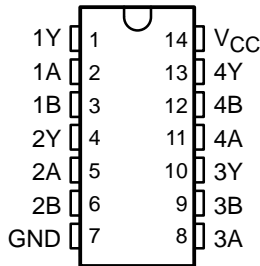


SN54AHCT02, SN74AHCT02 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

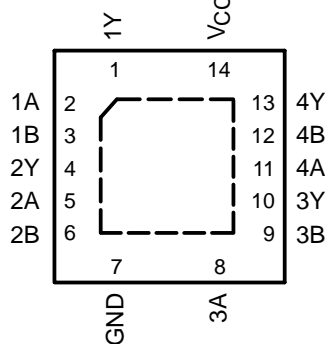
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- Inputs Are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

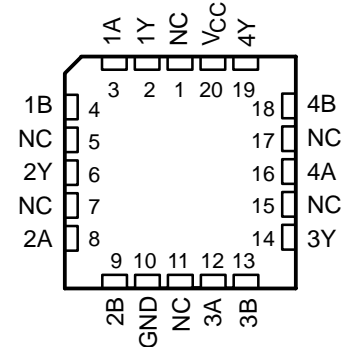
SN54AHCT02... J OR W PACKAGE
SN74AHCT02... D, DB, DGV, N, NS,
OR PW PACKAGE
(TOP VIEW)



SN74AHCT02... RGY PACKAGE
(TOP VIEW)



SN54AHCT02... FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

These devices contain four independent 2-input NOR gates that perform the Boolean function $Y = \overline{A} \cdot \overline{B}$ or $Y = \overline{A + B}$ in positive logic.

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Tape and reel	SN74AHCT02RGYR	HB02
	PDIP – N	Tube	SN74AHCT02N	SN74AHCT02N
	SOIC – D	Tube	SN74AHCT02D	AHCT02
		Tape and reel	SN74AHCT02DR	
	SOP – NS	Tape and reel	SN74AHCT02NSR	AHCT02
	SSOP – DB	Tape and reel	SN74AHCT02DBR	HB02
	TSSOP – PW	Tube	SN74AHCT02PW	HB02
Tape and reel		SN74AHCT02PWR		
–55°C to 125°C	TVSOP – DGV	Tape and reel	SN74AHCT02DGV	HB02
	CDIP – J	Tube	SNJ54AHCT02J	SNJ54AHCT02J
	CFP – W	Tube	SNJ54AHCT02W	SNJ54AHCT02W
	LCCC – FK	Tube	SNJ54AHCT02FK	SNJ54AHCT02FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

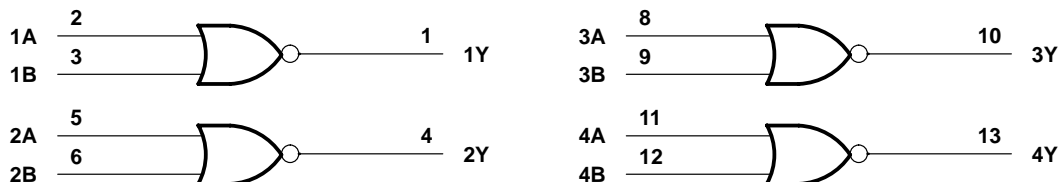
SN54AHCT02, SN74AHCT02 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

SCLS262L – DECEMBER 1995 – REVISED JULY 2003

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, RGY, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	86°C/W
(see Note 2): DB package	96°C/W
(see Note 2): DGV package	127°C/W
(see Note 2): N package	80°C/W
(see Note 2): NS package	76°C/W
(see Note 2): PW package	113°C/W
(see Note 3): RGY package	47°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.
 3. The package thermal impedance is calculated in accordance with JESD 51-5.



SN54AHCT02, SN74AHCT02 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

SCLS262L – DECEMBER 1995 – REVISED JULY 2003

recommended operating conditions (see Note 4)

		SN54AHCT02		SN74AHCT02		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		-8		-8	mA
I _{OL}	Low-level output current		8		8	mA
Δt/Δv	Input transition rise or fall rate		20		20	ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHCT02		SN74AHCT02		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4	4.5		4.4		4.4	V	
	I _{OH} = -8 mA		3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 μA	4.5 V			0.1			0.1	V	
	I _{OL} = 8 mA				0.36		0.44	0.44		
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1*	±1	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			2		20	20	μA	
ΔI _{CC} †	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V			1.35		1.5	1.5	mA	
C _i	V _I = V _{CC} or GND	5 V		4	10			10	pF	

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

† This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54AHCT02		SN74AHCT02		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	Y	C _L = 15 pF	2.4**	5.5**		1**	6.5**	1	6.5	ns
t _{PHL}				3.5**	5.5**		1**	6.5**	1	6.5	
t _{PLH}	A or B	Y	C _L = 50 pF	3.4	7.5		1	8.5	1	8.5	ns
t _{PHL}				4.5	7.5		1	8.5	1	8.5	

** On products compliant to MIL-PRF-38535, this parameter is not production tested.



SN54AHCT02, SN74AHCT02 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

SCLS262L – DECEMBER 1995 – REVISED JULY 2003

noise characteristics, $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER	SN74AHCT02			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$ Quiet output, minimum dynamic V_{OL}			-0.8	V
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}		4.7		V
$V_{IH(D)}$ High-level dynamic input voltage	2			V
$V_{IL(D)}$ Low-level dynamic input voltage			0.8	V

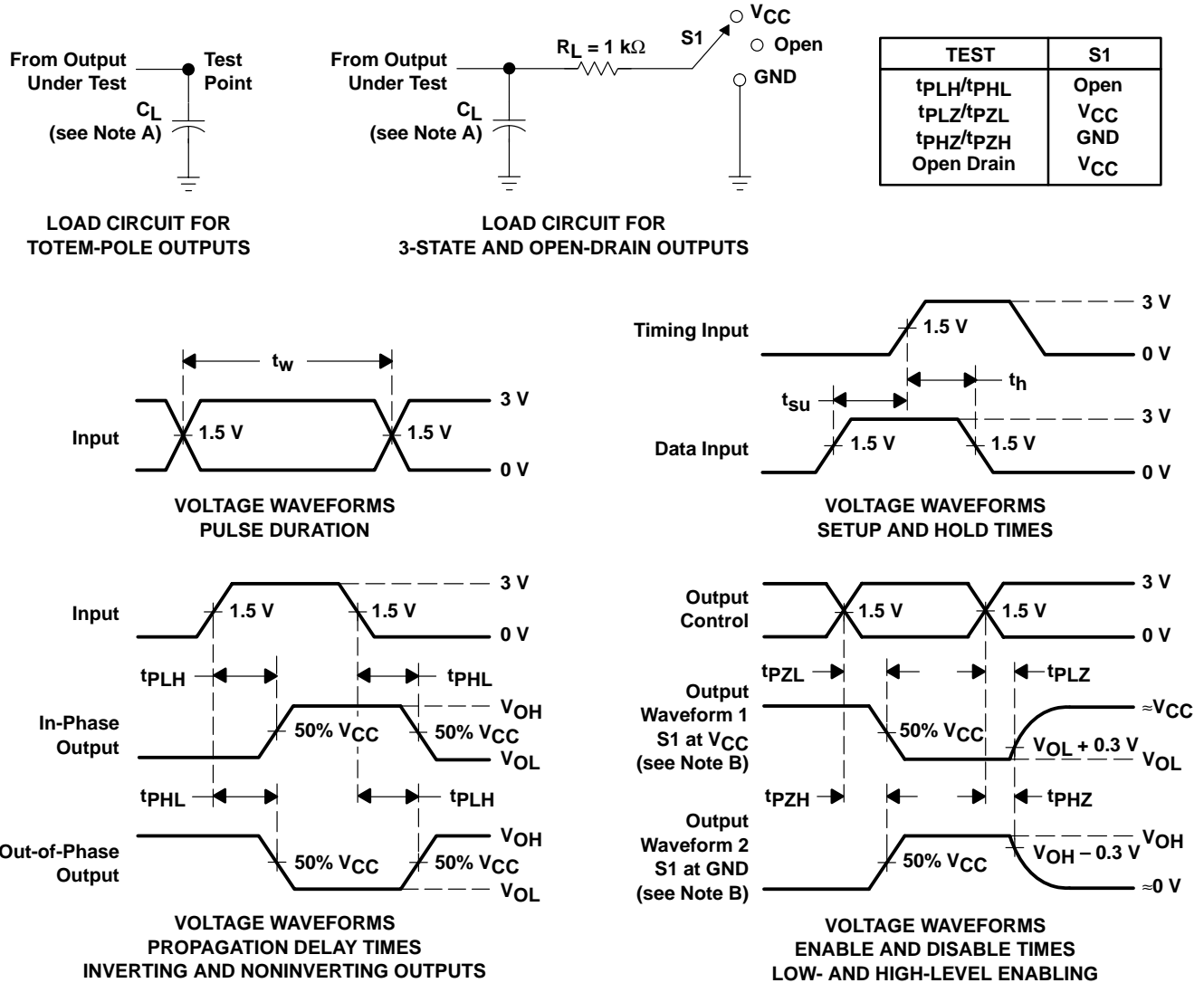
NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1\text{ MHz}$	17	pF



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is high except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is low except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms