FAIRCHILD SEMICONDUCTOR™

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# 74F283
# 4-Bit Binary Full Adder with Fast Carry

## General Description

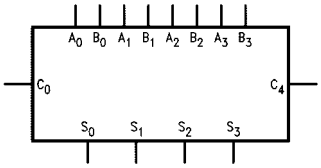
The 74F283 high-speed 4-bit binary full adder with internal carry lookahead accepts two 4-bit binary words ($A_0$–$A_3$, $B_0$–$B_3$) and a Carry input ($C_0$). It generates the binary Sum outputs ($S_0$–$S_3$) and the Carry output ($C_4$) from the most significant bit. The 74F283 will operate with either active HIGH or active LOW operands (positive or negative logic).

## Ordering Code:

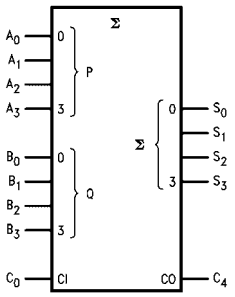
| Order Number | Package Number | Package Description |
|---|---|---|
| 74F283SC | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow |
| 74F283SJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74F283PC | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

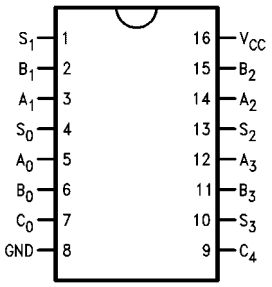
## Logic Symbols




IEEE/IEC




## Connection Diagram




## Unit Loading/Fan Out

| Pin Names | Description | U.L. HIGH/LOW | Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$ |
|---|---|---|---|
| $A_0$–$A_3$ | A Operand Inputs | 1.0/2.0 | 20 µA/–1.2 mA |
| $B_0$–$B_3$ | B Operand Inputs | 1.0/2.0 | 20 µA/–1.2 mA |
| $C_0$ | Carry Input | 1.0/1.0 | 20 µA/–0.6 mA |
| $S_0$–$S_3$ | Sum Outputs | 50/33.3 | –1 mA/20 mA |
| $C_4$ | Carry Output | 50/33.3 | –1 mA/20 mA |

## Functional Description

The 74F283 adds two 4-bit binary words (A plus B) plus the incoming Carry ($C_0$). The binary sum appears on the Sum ($S_0$–$S_3$) and outgoing carry ($C_4$) outputs. The binary weight of the various inputs and outputs is indicated by the subscript numbers, representing powers of two.

$$2^0 (A_0 + B_0 + C_0) + 2^1 (A_1 + B_1)$$
$$+ 2^2 (A_2 + B_2) + 2^3 (A_3 + B_3)$$
$$= S_0 + 2S_1 + 4S_2 + 8S_3 + 16C_4$$

Where (+) = plus

Interchanging inputs of equal weight does not affect the operation. Thus $C_0$, $A_0$, $B_0$ can be arbitrarily assigned to pins 5, 6 and 7 for DIPS, and 7, 8 and 9 for chip carrier packages. Due to the symmetry of the binary add function, the 74F283 can be used either with all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). See Figure 1. Note that if $C_0$ is not used it must be tied LOW for active HIGH logic or tied HIGH for active LOW logic.

Due to pin limitations, the intermediate carries of the 74F283 are not brought out for use as inputs or outputs. However, other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage. Figure 2 shows how to make a 3-bit adder. Tying the operand inputs of the fourth adder ($A_3$, $B_3$) LOW makes $S_3$ dependent only on, and equal to, the carry from the third adder. Using somewhat the same principle, Figure 3 shows a way of dividing the 74F283 into a 2-bit and a 1-bit adder. The third stage adder ($A_2$, $B_2$, $S_2$) is used merely as a means of getting a carry ($C_{10}$) signal into the fourth stage (via $A_2$ and $B_2$) and bringing out the carry from the second stage on $S_2$. Note that as long as $A_2$ and $B_2$ are the same, whether HIGH or LOW, they do not influence $S_2$. Similarly, when $A_2$ and $B_2$ are the same the carry into the third stage does not influence the carry out of the third stage. Figure 4 shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs $S_0$, $S_1$ and $S_2$ present a binary number equal to the number of inputs $I_1$–$I_5$ that are true. Figure 5 shows one method of implementing a 5-input majority gate. When three or more of the inputs $I_1$–$I_5$ are true, the output $M_5$ is true.

| | $C_0$ | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $B_0$ | $B_1$ | $B_2$ | $B_3$ | $S_0$ | $S_1$ | $S_2$ | $S_3$ | $C_4$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Logic Levels | L | L | H | L | H | H | L | L | H | H | H | L | L | H |
| Active HIGH | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| Active LOW | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

Active HIGH: 0 + 10 + 9 = 3 + 16  Active LOW: 1 + 5 + 6 = 12 + 0

**FIGURE 1. Active HIGH versus Active LOW Interpretation**

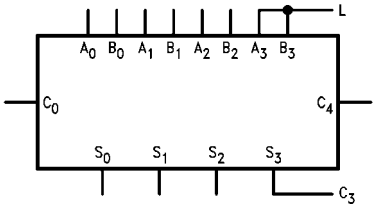



**FIGURE 2. 3-Bit Adder**

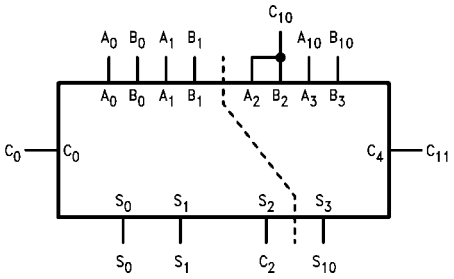



**FIGURE 3. 2-Bit and 1-Bit Adders**

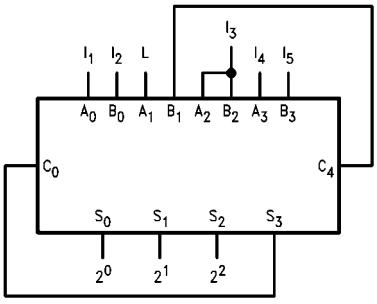



**FIGURE 4. 5-Input Encoder**

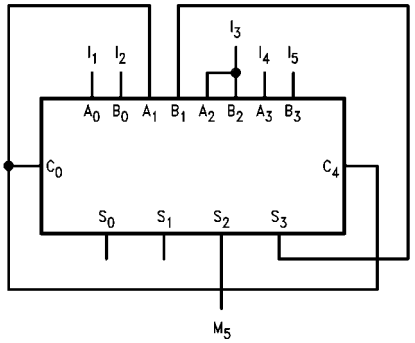
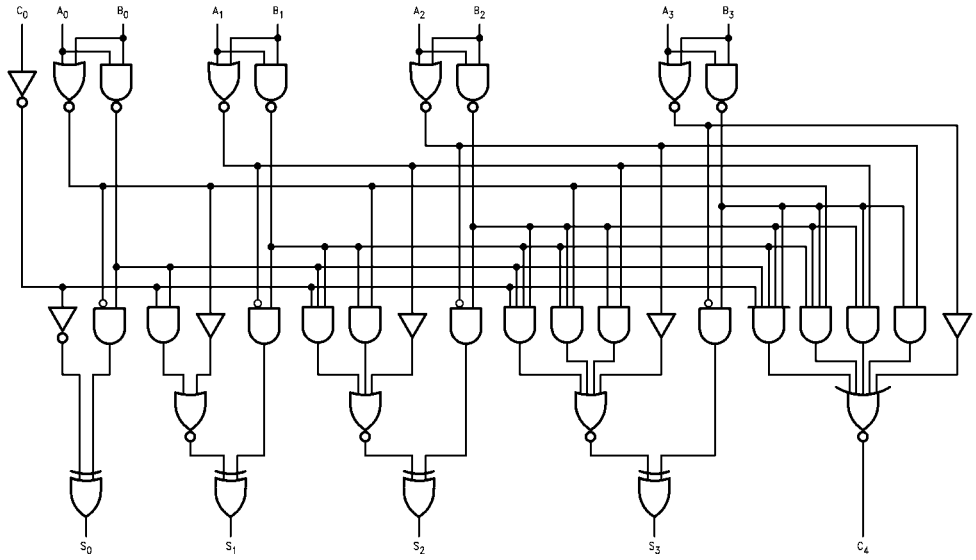



**FIGURE 5. 5-Input Majority Gate**

## Logic Diagram




Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings(Note 1)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature under Bias | −55°C to +125°C |
| Junction Temperature under Bias | −55°C to +150°C |
| $V_{CC}$ Pin Potential to Ground Pin | −0.5V to +7.0V |
| Input Voltage (Note 2) | −0.5V to +7.0V |
| Input Current (Note 2) | −30 mA to +5.0 mA |
| Voltage Applied to Output | |
| in HIGH State (with $V_{CC}$ = 0V) | |
| Standard Output | −0.5V to $V_{CC}$ |
| 3-STATE Output | −0.5V to +5.5V |
| Current Applied to Output | |
| in LOW State (Max) | twice the rated $I_{OL}$ (mA) |
| ESD Last Passing Voltage (Min) | 4000V |

## Recommended Operating Conditions

| | |
|---|---|
| Free Air Ambient Temperature | 0°C to +70°C |
| Supply Voltage | +4.5V to +5.5V |

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

| Symbol | Parameter | | Min | Typ | Max | Units | $V_{CC}$ | Conditions |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | V | | Recognized as a HIGH Signal |
| $V_{IL}$ | Input LOW Voltage | | | | 0.8 | V | | Recognized as a LOW Signal |
| $V_{CD}$ | Input Clamp Diode Voltage | | | | −1.2 | V | Min | $I_{IN}$ = −18 mA |
| $V_{OH}$ | Output HIGH | 10% $V_{CC}$ | 2.5 | | | V | Min | $I_{OH}$ = −1 mA |
| | Voltage | 5% $V_{CC}$ | 2.7 | | | | | $I_{OH}$ = −1 mA |
| $V_{OL}$ | Output LOW Voltage | 10% $V_{CC}$ | | | 0.5 | V | Min | $I_{OL}$ = 20 mA |
| $I_{IH}$ | Input HIGH Current | | | | 5.0 | µA | Max | $V_{IN}$ = 2.7V |
| $I_{BVI}$ | Input HIGH Current Breakdown Test | | | | 7.0 | µA | Max | $V_{IN}$ = 7.0V |
| $I_{CEX}$ | Output HIGH Leakage Current | | | | 50 | µA | Max | $V_{OUT}$ = $V_{CC}$ |
| $V_{ID}$ | Input Leakage Test | | 4.75 | | | V | 0.0 | $I_{ID}$ = 1.9 µA All Other Pins Grounded |
| $I_{OD}$ | Output Leakage Circuit Current | | | | 3.75 | µA | 0.0 | $V_{IOD}$ = 150 mV All Other Pins Grounded |
| $I_{IL}$ | Input LOW Current | | | | −0.6 | mA | Max | $V_{IN}$ = 0.5V ($C_O$) |
| | | | | | −1.2 | | | $V_{IN}$ = 0.5V ($A_n$, $B_n$) |
| $I_{OS}$ | Output Short-Circuit Current | | −60 | | −150 | mA | Max | $V_{OUT}$ = 0V |
| $I_{CCH}$ | Power Supply Current | | | 36 | 55 | mA | Max | $V_O$ = HIGH |
| $I_{CCL}$ | Power Supply Current | | | 36 | 55 | mA | Max | $V_O$ = LOW |

## AC Electrical Characteristics

| Symbol | Parameter | $T_A$ = +25°C, $V_{CC}$ = +5.0V, $C_L$ = 50 pF | | | $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V, $C_L$ = 50 pF | | $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V, $C_L$ = 50 pF | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Max | Min | Max | |
| $t_{PLH}$ | Propagation Delay | 3.5 | 7.0 | 9.5 | 3.5 | 14.0 | 3.5 | 11.0 | ns |
| $t_{PHL}$ | $C_0$ to $S_n$ | 3.0 | 7.0 | 9.5 | 3.0 | 14.0 | 3.0 | 11.0 | |
| $t_{PLH}$ | Propagation Delay | 3.0 | 7.0 | 9.5 | 3.0 | 17.0 | 3.0 | 13.0 | ns |
| $t_{PHL}$ | $A_n$ or $B_n$ to $S_n$ | 3.0 | 7.0 | 9.5 | 3.0 | 14.0 | 3.0 | 11.5 | |
| $t_{PLH}$ | Propagation Delay | 3.0 | 5.7 | 7.5 | 3.0 | 10.5 | 3.0 | 8.5 | ns |
| $t_{PHL}$ | $C_0$ to $C_4$ | 3.0 | 5.4 | 7.0 | 2.5 | 10.0 | 3.0 | 8.0 | |
| $t_{PLH}$ | Propagation Delay | 3.0 | 5.7 | 7.5 | 3.0 | 10.5 | 3.0 | 8.5 | ns |
| $t_{PHL}$ | $A_n$ or $B_n$ to $C_4$ | 2.5 | 5.3 | 7.0 | 2.5 | 10.0 | 2.5 | 8.0 | |