![Texas Instruments logo] **TEXAS INSTRUMENTS**

CD54HC4316, CD74HC4316, CD74HCT4316

High-Speed CMOS Logic
Quad Analog Switch with Level Translation

Features

- **Wide Analog-Input-Voltage Range**
  V_{CC} - V_{EE} . . . . **0V to 10V**

- **Low "ON" Resistance**
  - **45Ω (Typ)** . . . .**V_{CC} = 4.5V**
  - **35Ω (Typ)** . . . . **V_{CC} = 6V**
  - **30Ω (Typ)** . . . . **V_{CC} - V_{EE} = 9V**

- **Fast Switching and Propagation Delay Times**

- **Low "OFF" Leakage Current**

- **Built-In "Break-Before-Make" Switching**

- **Logic-Level Translation to Enable 5V Logic to Accommodate ±5V Analog Signals**

- **Wide Operating Temperature Range . . . -55°C to 125°C**

- **HC Types**
  - **2V to 10V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**

- **HCT Types**
  - **Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

Description

The 'HC4316 and CD74HCT4316 contain four independent digitally controlled analog switches that use silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

In addition these devices contain logic-level translation circuits that provide for analog signal switching of voltages between ±5V via 5V logic. Each switch is turned on by a high-level voltage on its select input (S) when the common Enable (E) is Low. A High E disables all switches. The digital inputs can swing between V_{CC} and GND; the analog inputs/outputs can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. Voltage ranges are shown in Figures 2 and 3.

Ordering Information

| PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC4316F3A	-55 to 125	16 Ld CERDIP
CD74HC4316E	-55 to 125	16 Ld PDIP
CD74HC4316M	-55 to 125	16 Ld SOIC
CD74HC4316MT	-55 to 125	16 Ld SOIC
CD74HC4316M96	-55 to 125	16 Ld SOIC
CD74HC4316NSR	-55 to 125	16 Ld SOP
CD74HC4316PW	-55 to 125	16 Ld TSSOP
CD74HC4316PWR	-55 to 125	16 Ld TSSOP
CD74HC4316PWT	-55 to 125	16 Ld TSSOP
CD74HCT4316E	-55 to 125	16 Ld PDIP
CD74HCT4316M	-55 to 125	16 Ld SOIC
CD74HCT4316MT	-55 to 125	16 Ld SOIC
CD74HCT4316M96	-55 to 125	16 Ld SOIC

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

Pinout

CD54HC4316 (CERDIP)
CD74HC4316 (PDIP, SOIC, SOP, TSSOP)
CD74HCT4316 (PDIP, SOIC)
TOP VIEW

Pin			Pin
1Z	1	16	V_{CC}
1Y	2	15	1S
2Y	3	14	4S
2Z	4	13	4Z
2S	5	12	4Y
3S	6	11	3Y
$\overline{E}$	7	10	3Z
GND	8	9	V_{EE}

Functional Diagram

V_{CC}

16

15 1S

5 2S

6 3S

14 4S

$\overline{E}$ 7

LOGIC
LEVEL
CONV.
AND
CONTROL

2 1Y
1 1Z
3 2Y
4 2Z
11 3Y
10 3Z
12 4Y
13 4Z

8 9
GND V_{EE}
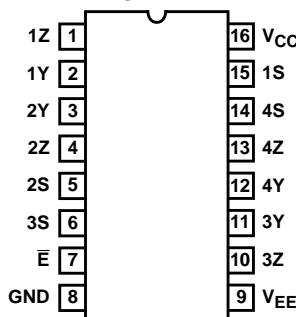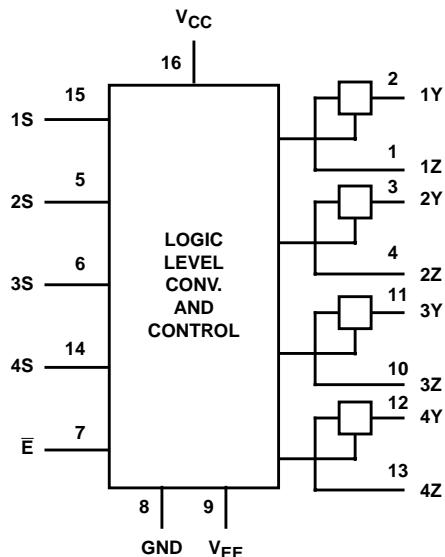
TRUTH TABLE

INPUTS		
$\overline{E}$	S	SWITCH
L	L	OFF
L	H	ON
H	X	OFF

H= High Level Voltage
L= Low Level Voltage
X= Don't Care

Logic Diagram

TO 3 OTHER
SWITCHES

nY

V_{CC}

LOGIC
LEVEL
CONV.

V_{CC}

$\overline{E}$

nZ

V_{EE}

V_{EE}

nS
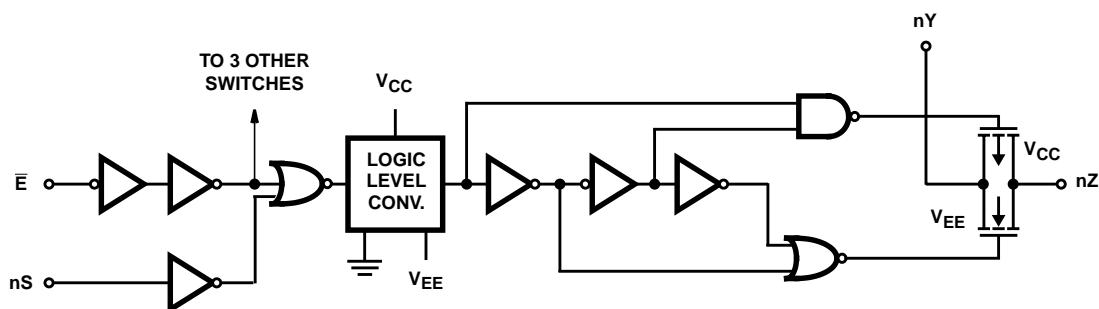
FIGURE 1. ONE SWITCH

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . -0.5V to 7V
DC Supply Voltage, V_{CC} - V_{EE}. . . . . -0.5V to 10.5V
DC Supply Voltage, V_{EE} . . . . 0.5V to -7V
DC Input Diode Current, I_{IK}
   For V_I < -0.5V or V_I > V_{CC} 0.5V. . . . .±20mA
DC Switch Diode Current, I_{OK}
   For V_I < V_{EE} -0.5V or V_I < V_{CC} + 0.5V . . . .±25mA
DC Switch Diode Current
   For V_I > V_{EE} -0.5V or V_I < V_{CC} + 0.5V . . . .±25mA
DC Output Diode Current, I_{OK}
   For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . .±20mA
DC Output Source or Sink Current per Output Pin, I_O
   For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . .±25mA
DC V_{CC} or Ground Current, I_{CC} . . . .±50mA

Operating Conditions

Temperature Range, T_A . . . . -55°C to 125°C
Supply Voltage Range, V_{CC}
   HC Types . . . . .2V to 6V
   HCT Types . . . . .4.5V to 5.5V
Supply Voltage Range, V_{CC} - V_{EE}
   HC, HCT Types (Figure 2) . . . . .2V to 10V
Supply Voltage Range, V_{EE}
   HC, HCT Types (Figure 3) . . . . 0V to -6V
DC Input or Output Voltage, V_I . . . . GND to V_{CC}
Analog Switch I/O Voltage, V_{IS}. . . . . V_{EE} (Min)
. . . . V_{CC} (Max)
Input Rise and Fall Time, t_r, t_f
   2V . . . . 1000ns (Max)
   4.5V. . . . . 500ns (Max)
   6V . . . . 400ns (Max)

Thermal Information

Package Thermal Impedance, θ_{JA} (see Note 1):
   E (PDIP) Package . . . . .67°C/W
   M (SOIC) Package. . . . . .73°C/W
   NS (SOP) Package . . . . .64°C/W
   PW (TSSOP) Package . . . . .108°C/W
Maximum Junction Temperature (Plastic Package) . . . . 150°
Maximum Storage Temperature Range . . . . -65°C to 150°
Maximum Lead Temperature (Soldering 10s) . . . . 300°
   SOIC - Lead Tips Only

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Area as a Function of Supply Voltage
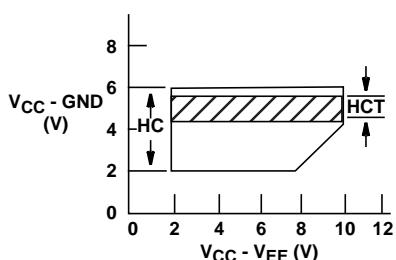
FIGURE 2.
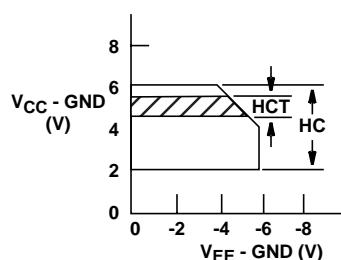
FIGURE 3.

CD54HC4316, CD74HC4316, CD74HCT4316

DC Electrical Specifications

PARAMETER	SYMBOL	V_I (V)	V_{IS} (V)	V_{EE} (V)	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
						MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES													
High Level Input Voltage	V_{IH}	-	-	-	2	1.5	-	-	1.5	-	1.5	-	V
					4.5	3.15	-	-	3.15	-	3.15	-	V
					6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	-	2	-	-	0.5	-	0.5	-	0.5	V
					4.5	-	-	1.35	-	1.35	-	1.35	V
					6	-	-	1.8	-	1.8	-	1.8	V
"ON" Resistance I_O = 1mA (Figures 4, 5)	R_{ON}	V_{IH} or V_{IL}	V_{CC} or V_{EE}	0	4.5	-	45	180	-	225	-	270	Ω
				0	6	-	35	160	-	200	-	240	Ω
				-4.5	4.5	-	30	135	-	170	-	205	Ω
			V_{CC} to V_{EE}	0	4.5	-	85	320	-	400	-	480	Ω
				0	6	-	55	240	-	300	-	360	Ω
				-4.5	4.5	-	35	170	-	215	-	255	Ω
Maximum "ON" Resistance Between Any Two Channels	ΔR_{ON}	-	-	0	4.5	-	10	-	-	-	-	-	Ω
				0	6	-	8.5	-	-	-	-	-	Ω
				-4.5	4.5	-	5	-	-	-	-	-	Ω
Switch Off Leakage Current	I_{IZ}	V_{IH} or V_{IL}	V_{CC} - V_{EE}	0	6	-	-	±0.1	-	±1	-	±1	µA
				-5	5	-	-	±0.1	-	±1	-	±1	µA
Control Input Leakage Current	I_{IL}	V_{CC} or GND	-	0	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current I_O = 0	I_{CC}	V_{CC} or GND	When V_{IS} = V_{EE}, V_{OS}=V_{CC} When V_{IS}=V_{CC}, V_{OS}=V_{EE}	0	6	-	-	8	-	80	-	160	µA
				-5	5	-	-	16	-	160	-	320	µA
HCT TYPES													
High Level Input Voltage	V_{IH}	-	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
"ON" Resistance I_O = 1mA (Figures 4, 5)	R_{ON}	V_{IH} or V_{IL}	V_{CC} or V_{EE}	0	4.5	-	45	180	-	225	-	270	Ω
				-4.5	4.5	-	30	135	-	170	-	205	Ω
			V_{CC} to V_{EE}	0	4.5	-	85	320	-	400	-	480	Ω
				-4.5	4.5	-	35	170	-	215	-	255	Ω
Maximum "ON" Resistance Between Any Two Channels	ΔR_{ON}	-	-	0	4.5	-	10	-	-	-	-	-	Ω
				-4.5	4.5	-	5	-	-	-	-	-	Ω
Switch Off Leakage Current	I_{IZ}	V_{IH} or V_{IL}	V_{CC} - V_{EE}	0	6	-	-	±0.1	-	±1	-	±1	µA
				-5	5	-	-	±0.1	-	±1	-	±1	µA

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	V_I (V)	V_{IS} (V)	V_{EE} (V)	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
			TEST CONDITIONS				25°C		-40°C TO 85°C		-55°C TO 125°C		
Control Input Leakage Current	I_I	V_{CC} or GND	-	0	5.5	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current $I_O = 0$	I_{CC}	Any Voltage Between V_{CC} and GND	When $V_{IS} = V_{EE}$, $V_{OS} = V_{CC}$, When $V_{IS} = V_{CC}$, $V_{OS} = V_{EE}$	0	5.5	-	-	8	-	80	-	160	µA
				-4.5	5.5	-	-	16	-	160	-	320	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC} (Note 2)	V_{CC} -2.1	-	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTE:

2. For dual-supply systems theoretical worst case ($V_I = 2.4V$, $V_{CC} = 5.5V$) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
All	0.5

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g., 360µA max at 25°C.

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{EE} (V)	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
						25°C		-40°C TO 85°C		-55°C TO 125°C		
HC TYPES												
Propagation Delay, Switch In to Out	t_{PLH}, t_{PHL}	$C_L = 50pF$	0	2	-	-	60	-	75	-	90	ns
			0	4.5	-	-	12	-	15	-	18	ns
			0	6	-	-	10	-	13	-	15	ns
			-4.5	4.5	-	-	8	-	10	-	12	ns
Turn "ON" Time $\overline{E}$ to Out	t_{PZH}, t_{PZL}	$C_L = 50pF$	0	2	-	-	205	-	255	-	310	ns
			0	4.5	-	-	41	-	51	-	62	ns
			0	6	-	-	35	-	43	-	53	ns
			-4.5	4.5	-	-	37	-	47	-	56	ns
		$C_L = 15pF$	-	5	-	17	-	-	-	-	-	ns
Turn "ON" Time nS to Out	t_{PZH}, t_{PZL}	$C_L = 50pF$	0	2	-	-	175	-	220	-	265	ns
			0	4.5	-	-	35	-	44	-	53	ns
			0	6	-	-	30	-	37	-	45	ns
			-4.5	4.5	-	-	34	-	43	-	51	ns
		$C_L = 15pF$	-	5	-	14	-	-	-	-	-	ns
Turn "OFF" Time $\overline{E}$ to Out	t_{PLZ}, t_{PHZ}	$C_L = 50pF$	0	2	-	-	205	-	255	-	310	ns
			0	4.5	-	-	41	-	51	-	62	ns
			0	6	-	-	35	-	43	-	53	ns
			-4.5	4.5	-	-	37	-	47	-	56	ns
		$C_L = 15pF$	-	5	-	17	-	-	-	-	-	ns

Switching Specifications Input t_r, t_f = 6ns (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V_{EE} (V)	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Turn "OFF" Time nS to Out	t_{PLZ}, t_{PHZ}	C_L = 50pF	0	2	-	-	175	-	220	-	265	ns
			0	4.5	-	-	35	-	44	-	53	ns
			0	6	-	-	30	-	37	-	45	ns
			-4.5	4.5	-	-	34	-	43	-	51	ns
		C_L = 15pF	-	5	-	14	-	-	-	-	-	ns
Input (Control) Capacitance	C_I	-	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C_{PD}	-	-	5	-	42	-	-	-	-	-	pF
HCT TYPES												
Propagation Delay, Switch In to Switch Out	t_{PLH}, t_{PHL}	C_L = 50pF	0	4.5	-	-	12	-	15	-	18	ns
			-4.5	4.5	-	-	8	-	10	-	12	ns
Turn "ON" Time $\overline{E}$ to Out	t_{PZH}	C_L = 50pF	0	4.5	-	-	44	-	55	-	66	ns
			-4.5	4.5	-	-	42	-	53	-	63	ns
		C_L = 15pF	-	5	-	18	-	-	-	-	-	ns
	t_{PZL}	C_L = 50pF	0	4.5	-	-	56	-	70	-	85	ns
			-4.5	4.5	-	-	42	-	53	-	63	ns
		C_L = 15pF	-	5	-	24	-	-	-	-	-	ns
Turn "ON" Time nS to Out	t_{PZH}	C_L = 50pF	0	4.5	-	-	40	-	53	-	60	ns
			-4.5	4.5	-	-	34	-	43	-	51	ns
		C_L = 15pF	-	5	-	17	-	-	-	-	-	ns
	t_{PZL}	C_L = 50pF	0	4.5	-	-	50	-	63	-	75	ns
			-4.5	4.5	-	-	34	-	43	-	51	ns
		C_L = 15pF	-	5	-	18	-	-	-	-	-	ns
Turn "OFF" Time $\overline{E}$ to Out	t_{PLZ}	C_L = 50pF	0	4.5	-	-	50	-	63	-	75	ns
			-4.5	4.5	-	-	46	-	58	-	69	ns
	t_{PLZ}, t_{PHZ}	C_L = 15pF	-	5	-	21	-	-	-	-	-	ns
Turn "OFF" Time nS to Out	t_{PHZ}	C_L = 50pF	0	4.5	-	-	44	-	55	-	66	ns
			-4.5	4.5	-	-	40	-	50	-	60	ns
	t_{PLZ}, t_{PHZ}	C_L = 15pF	-	5	-	18	-	-	-	-	-	ns
Input (Control) Capacitance	C_I	-	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C_{PD}	-	-	5	-	47	-	-	-	-	-	pF

NOTES:

3. C_{PD} is used to determine the dynamic power consumption, per package.

4. $P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L + C_S) V_{CC}^2 f_o$ where f_i = input frequency, f_o = output frequency, C_L = output load capacitance, C_S = switch capacitance, V_{CC} = supply voltage.

Analog Channel Specifications T_A = 25°C

PARAMETER	TEST CONDITIONS	V_{CC} (V)	HC4316	CD74HCT4316	UNITS
Switch Frequency Response Bandwidth at -3dB (Figure 6)	Figure 9 (Notes 5, 6)	4.5	>200	>200	MHz
Crosstalk Between Any Two Switches (Figure 7)	Figure 8 (Notes 6, 7)	4.5	TBE	TBE	dB

Analog Channel Specifications $T_A = 25^oC$ **(Continued)**

PARAMETER	TEST CONDITIONS	V_{CC} (V)	HC4316	CD74HCT4316	UNITS
Total Harmonic Distortion	1kHz, $V_{IS} = 4V_{P-P}$ (Figure 10)	4.5	0.078	0.078	%
	1kHz, $V_{IS} = 8V_{P-P}$ (Figure 10)	9	0.018	0.018	%
Control to Switch Feedthrough Noise	Figure 11	4.5	TBE	TBE	mV
		9	TBE	TBE	mV
Switch "OFF" Signal Feedthrough (Figure 7)	Figure 12 (Notes 6, 7)	4.5	-62	-62	dB
Switch Input Capacitance, C_S	-	-	5	5	pF

NOTES:

5. Adjust input level for 0dBm at output, f = 1MHz.

6. V_{IS} is centered at $V_{CC}/2$.

7. Adjust input for 0dBm at V_{IS}.

Typical Performance Curves
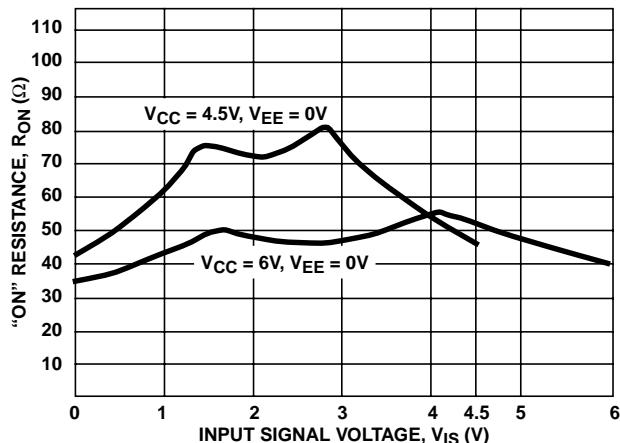
FIGURE 4. TYPICAL "ON" RESISTANCE vs INPUT SIGNAL VOLTAGE
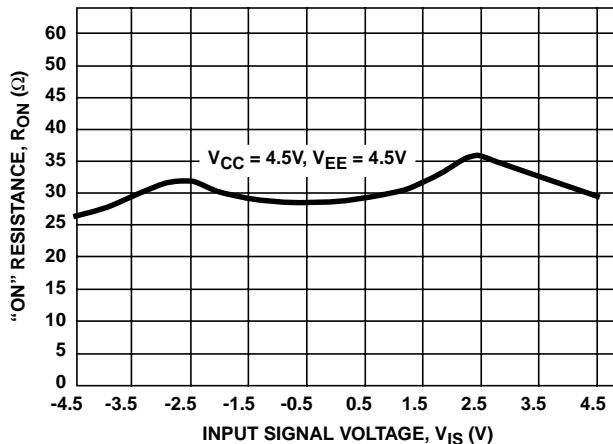
FIGURE 5. TYPICAL "ON" RESISTANCE vs INPUT SIGNAL VOLTAGE
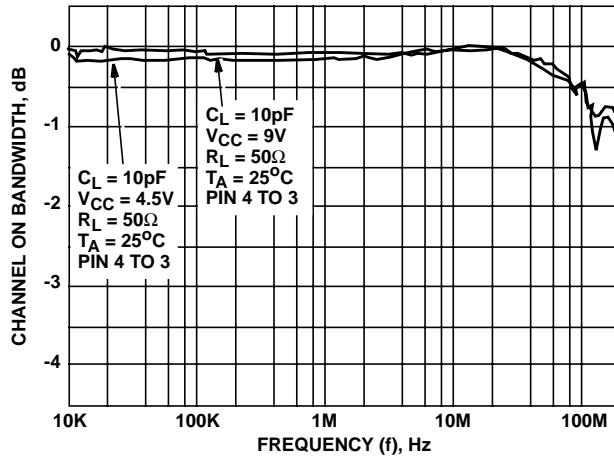
FIGURE 6. SWITCH FREQUENCY RESPONSE
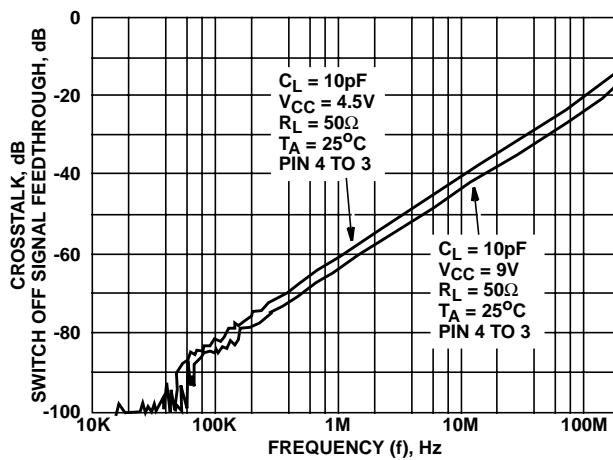
FIGURE 7. SWITCH-OFF SIGNAL FEEDTHROUGH AND CROSSTALK vs FREQUENCY

Analog Test Circuits

f_{IS} = 1MHz SINEWAVE
R = 50Ω
C = 10pF
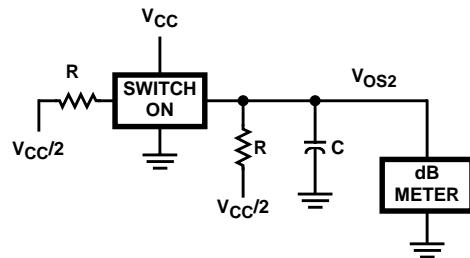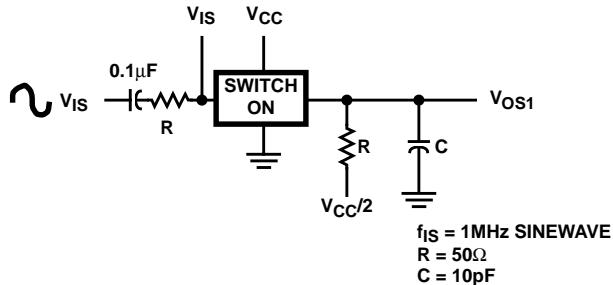
FIGURE 8. CROSSTALK BETWEEN TWO SWITCHES TEST CIRCUIT
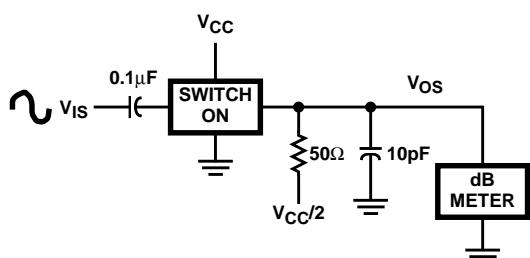
FIGURE 9. FREQUENCY RESPONSE TEST CIRCUIT

f_{IS} = 1kHz TO 10kHz
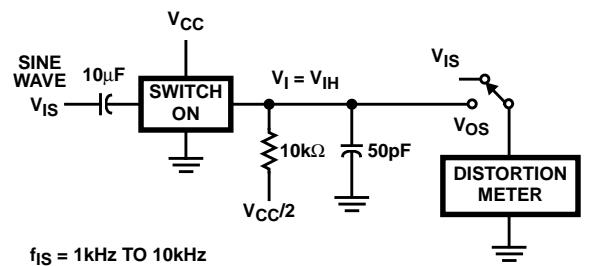
FIGURE 10. TOTAL HARMONIC DISTORTION TEST CIRCUIT
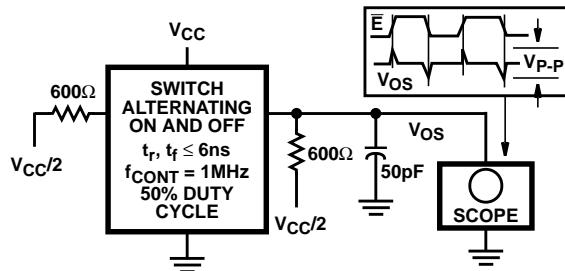
FIGURE 11. CONTROL-TO-SWITCH FEEDTHROUGH NOISE TEST CIRCUIT

$f_{IS} \geq$ 1MHz SINEWAVE
R = 50Ω
C = 10pF
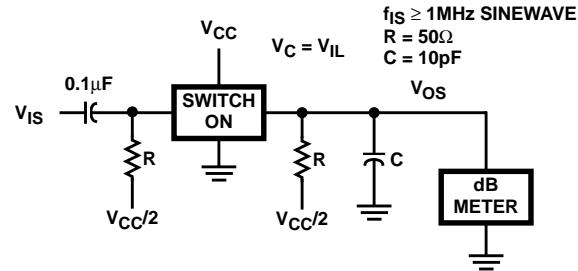
FIGURE 12. SWITCH OFF SIGNAL FEEDTHROUGH

8

## *Test Circuits and Waveforms*
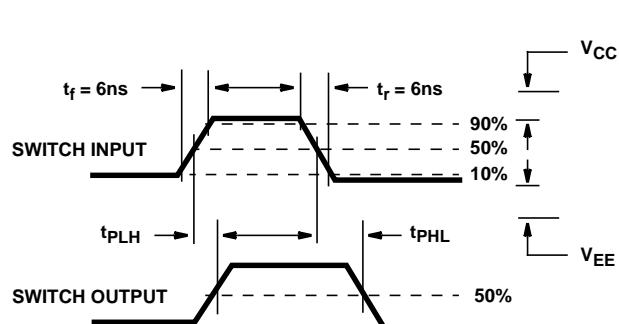

FIGURE 13. SWITCH PROPAGATION DELAY TIMES
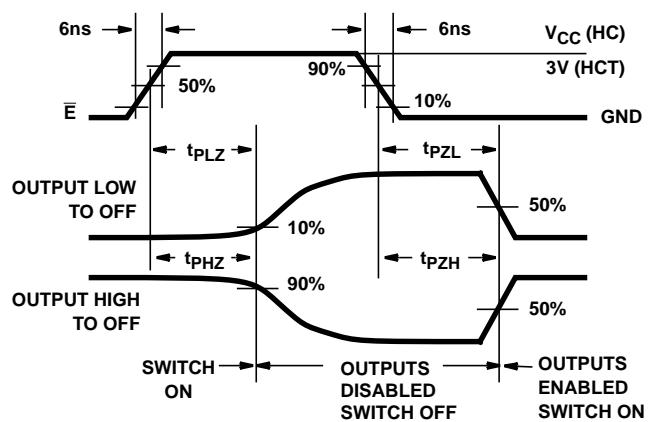
FIGURE 14. SWITCH TURN-ON AND TURN-OFF PROPAGATION DELAY TIMES WAVEFORMS