TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS143C

November 1997 - Revised August 2003

High-Speed CMOS Logic
Quad Buffer, Three-State

Features

- **Three-State Outputs**
- **Separate Output Enable Inputs**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs** . . . . **10 LSTTL Loads**
  - **Bus Driver Outputs** . . . . **15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55°C to 125°C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL} = 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

Description

The 'HC125 and 'HCT125 contain 4 independent three-state buffers, each having its own output enable input, which when "HIGH" puts the output in the high impedance state.
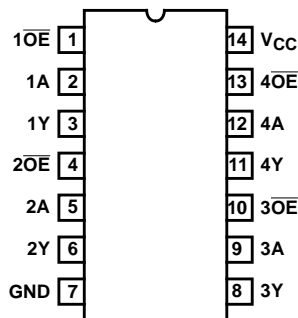
Ordering Information

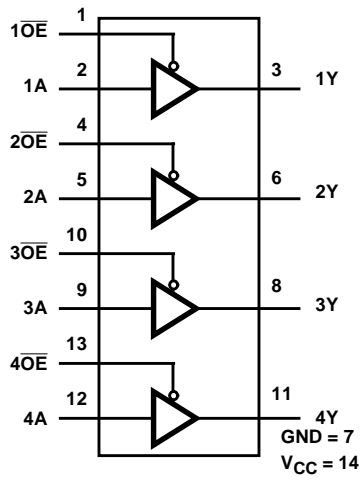| PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE
CD54HC125F3A	-55 to 125	14 Ld CERDIP
CD54HCT125F3A	-55 to 125	14 Ld CERDIP
CD74HC125E	-55 to 125	14 Ld PDIP
CD74HC125M	-55 to 125	14 Ld SOIC
CD74HC125MT	-55 to 125	14 Ld SOIC
CD74HC125M96	-55 to 125	14 Ld SOIC
CD74HCT125E	-55 to 125	14 Ld PDIP
CD74HCT125M	-55 to 125	14 Ld SOIC
CD74HCT125MT	-55 to 125	14 Ld SOIC
CD74HCT125M96	-55 to 125	14 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

Pinout

CD54HC125, CD54HCT125
(CERDIP)
CD74HC125, CD74HCT125
(PDIP, SOIC)
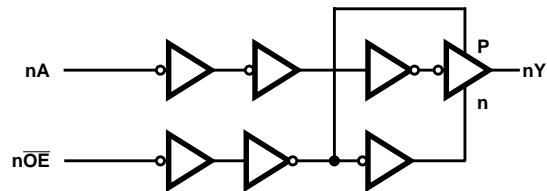TOP VIEW

1$\overline{OE}$	1	14	V_{CC}
1A	2	13	4$\overline{OE}$
1Y	3	12	4A
2$\overline{OE}$	4	11	4Y
2A	5	10	3$\overline{OE}$
2Y	6	9	3A
GND	7	8	3Y

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Functional Diagram

1$\overline{OE}$	1			
1A	2		3	1Y
2$\overline{OE}$	4			
2A	5		6	2Y
3$\overline{OE}$	10			
3A	9		8	3Y
4$\overline{OE}$	13			
4A	12		11	4Y

GND = 7
V_{CC} = 14

TRUTH TABLE

INPUTS		OUTPUTS
nA	n$\overline{OE}$	nY
H	L	H
L	L	L
X	H	Z

H= High Voltage Level
L= Low Voltage Level
X= Don't Care
Z= High Impedance, OFF State

Logic Diagram

nA ——

n$\overline{OE}$ ——

P

n

nY

CD54HC125, CD74HC125, CD54HCT125, CD74HCT125

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
  For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . .±20mA
DC Output Diode Current, I_{OK}
  For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . .±20mA
DC Drain Current, per Output, I_O
  For -0.5V < V_O < V_{CC} + 0.5V . . . .±35mA
DC Output Source or Sink Current per Output Pin, I_O
  For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . .±25mA
DC V_{CC} or Ground Current, I_{CC} . . . .±70mA

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (^oC/W)
E (PDIP) Package	80
M (SOIC) Package.	86

Maximum Junction Temperature . . . . .150^oC
Maximum Storage Temperature Range . . . .-65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . .300^oC
  (SOIC - Lead Tips Only)

Operating Conditions

Temperature Range (T_A) . . . . -55^oC to 125^oC
Supply Voltage Range, V_{CC}
  HC Types . . . . .2V to 6V
  HCT Types . . . . .4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . 0V to V_{CC}
Input Rise and Fall Time
  2V . . . . 1000ns (Max)
  4.5V. . . . . 500ns (Max)
  6V . . . . 400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	25^oC MIN	25^oC TYP	25^oC MAX	-40^oC TO 85^oC MIN	-40^oC TO 85^oC MAX	-55^oC TO 125^oC MIN	-55^oC TO 125^oC MAX	UNITS
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-6	4.5	3.98	-	-	3.84	-	3.7	-	V
			-7.8	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			6	4.5	-	-	0.26	-	0.33	-	0.4	V
			7.8	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA

DC Electrical Specifications   (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS			25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)	V_{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	µA
Three-State Leakage Current	I_{OZ}	V_{IL} or V_{IH}	-	6	-	-	±0.5	-	±5	-	±10	µA
HCT TYPES												
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-6	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			6	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} to GND	0	5.5	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	5.5	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC} (Note 2)	V_{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA
Three-State Leakage Current	I_{OZ}	V_{IL} or V_{IH}	-	5.5	-	-	±0.5	-	±5	-	±10	µA

NOTE:

2. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
nA, n$\overline{OE}$	1

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g., 360µA max at 25°C.

CD54HC125, CD74HC125, CD54HCT125, CD74HCT125

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C		-40°C TO 85°C	-55°C TO 125°C	UNITS
				TYP	MAX	MAX	MAX	
HC TYPES								
Propagation Delay Time nA to nY	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	100	125	150	ns
			4.5	-	20	25	30	ns
		C_L = 15pF	5	8	-	-	-	ns
		CL = 50pF	6	-	17	21	26	ns
Enable Delay Time	t_{PZL}, t_{PZH}	C_L = 50pF	2	-	125	155	190	ns
			4.5	-	25	31	38	ns
		C_L = 15pF	5	10	-	-	-	ns
		CL = 50pF	6	-	21	26	32	ns
Disable Delay Time	t_{PLZ}, t_{PHZ}	C_L = 50pF	2	-	125	155	190	ns
		C_L = 50pF	4.5	-	25	31	38	ns
		C_L = 15pF	5	10	-	-	-	ns
		C_L = 50pF	6	-	21	26	32	ns
Output Transition Time	t_{TLH}, t_{THL}	C_L = 50pF	2	-	60	75	90	ns
			4.5	-	12	15	18	ns
			6	-	10	13	15	ns
Input Capacitance	C_I	-	-	-	10	10	10	pF
Three-State Output Capacitance	C_O	-	-	-	20	20	20	pF
Power Dissipation Capacitance (Notes 3, 4)	C_{PD}	-	5	29	-	-	-	pF
HCT TYPES								
Propagation Delay Time nA to nY	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	25	31	38	ns
		C_L = 15pF	5	10	-	-	-	ns
Output Enable Time	t_{PZL}, t_{PZH}	C_L = 50pF	4.5	-	25	31	38	ns
		C_L = 15pF	5	10	-	-	-	ns
Output Disabling Time	t_{PLZ}, t_{PHZ}	C_L = 50pF	4.5	-	28	35	42	ns
		C_L = 15pF	5	11	-	-	-	ns
Output Transition Times	t_{TLH}, t_{THL}	C_L = 50pF	4.5	-	12	15	18	ns
Input Capacitance	C_I	-	-	-	10	10	10	pF
Three-State Output Capacitance	C_O	-	-	-	20	20	20	pF
Power Dissipation Capacitance (Notes 3, 4)	C_{PD}	-	5	34	-	-	-	pF

NOTES:

3. C_{PD} is used to determine the dynamic power consumption, per channel.

4. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, f_O = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.
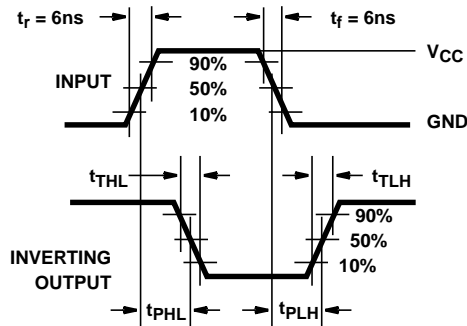
Test Circuits and Waveforms

FIGURE 1. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC
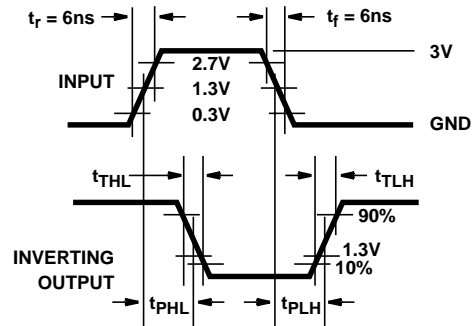
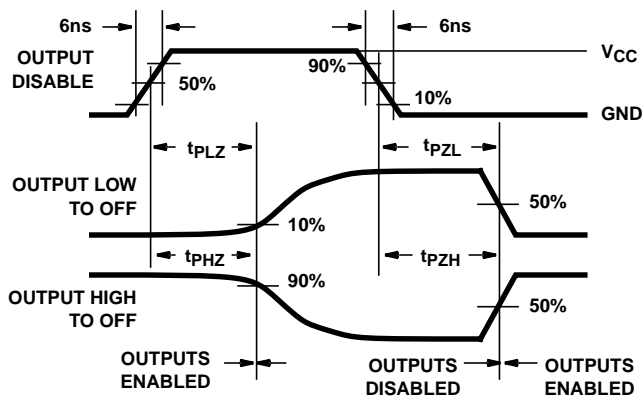**FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**

FIGURE 3. HC THREE-STATE PROPAGATION DELAY WAVEFORM
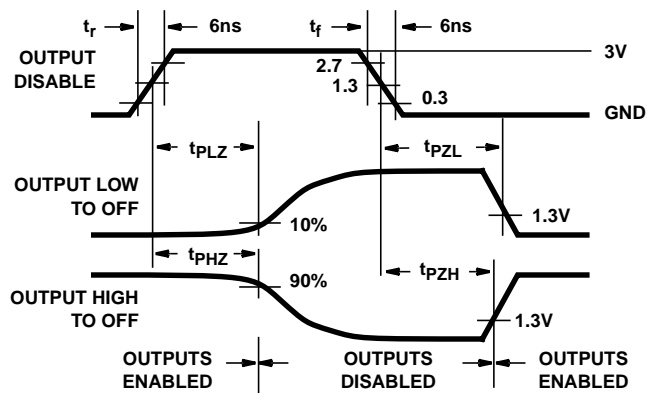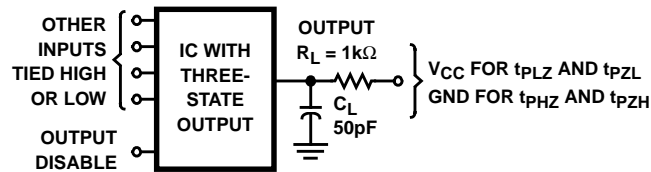
FIGURE 4. HCT THREE-STATE PROPAGATION DELAY WAVEFORM

NOTE: Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is Output R_L = 1kΩ to V_{CC}, C_L = 50pF.

FIGURE 5. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT