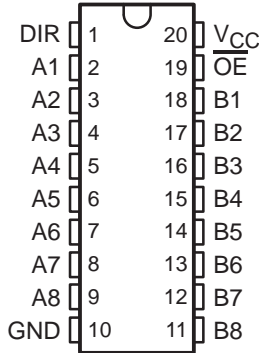


SN54AHCT245, SN74AHCT245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

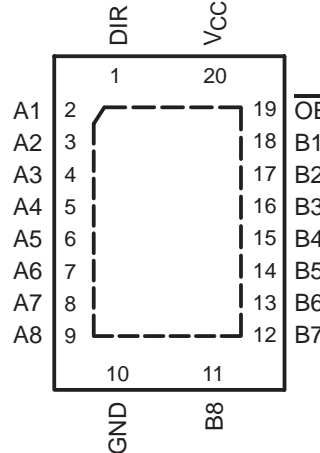
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- Inputs Are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

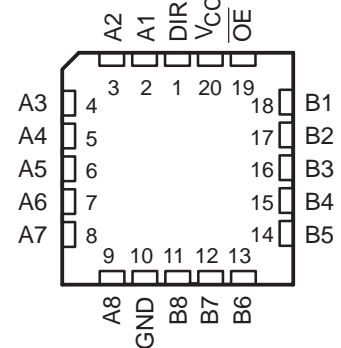
SN54AHCT245 . . . J OR W PACKAGE
SN74AHCT245 . . . DB, DGV, DW, N, NS,
OR PW PACKAGE
(TOP VIEW)



SN74AHCT245 . . . RGY PACKAGE
(TOP VIEW)



SN54AHCT245 . . . FK PACKAGE
(TOP VIEW)



description/ordering information

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

The 'AHCT245 devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses effectively are isolated.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74AHCT245N	SN74AHCT245N
	QFN – RGY	Tape and reel	SN74AHCT245RGYR	HB245
	SOIC – DW	Tube	SN74AHCT245DW	AHCT245
		Tape and reel	SN74AHCT245DWR	
	SOP – NS	Tape and reel	SN74AHCT245NSR	AHCT245
	SSOP – DB	Tape and reel	SN74AHCT245DBR	HB245
	TSSOP – PW	Tube	SN74AHCT245PW	HB245
Tape and reel		SN74AHCT245PWR		
–55°C to 125°C	TVSOP – DGV	Tape and reel	SN74AHCT245DGVR	HB245
	CDIP – J	Tube	SNJ54AHCT245J	SNJ54AHCT245J
	CFP – W	Tube	SNJ54AHCT245W	SNJ54AHCT245W
	LCCC – FK	Tube	SNJ54AHCT245FK	SNJ54AHCT245FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

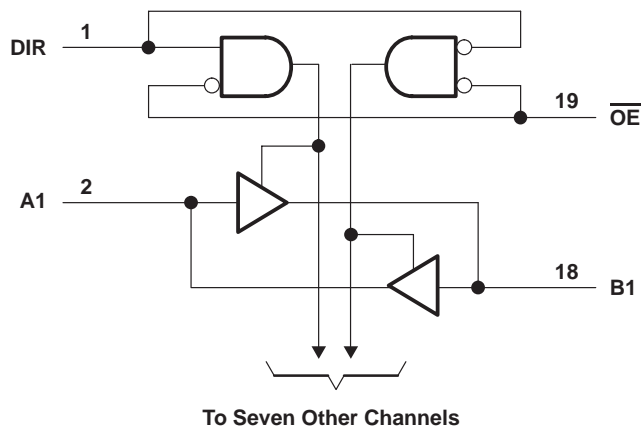
SN54AHCT245, SN74AHCT245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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FUNCTION TABLE
(each transceiver)

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1): Control inputs	-0.5 V to 7 V
I/O, Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$): Control inputs	-20 mA
I/O, Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 75 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package	70°C/W
(see Note 2): DGV package	92°C/W
(see Note 2): DW package	58°C/W
(see Note 2): N package	69°C/W
(see Note 2): NS package	60°C/W
(see Note 2): PW package	83°C/W
(see Note 3): RGY package	37°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. The package thermal impedance is calculated in accordance with JESD 51-5.

SN54AHCT245, SN74AHCT245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

	SN54AHCT245		SN74AHCT245		UNIT
	MIN	MAX	MIN	MAX	
V _{CC} Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH} High-level input voltage	2		2		V
V _{IL} Low-level input voltage		0.8		0.8	V
V _I Input voltage	0	5.5	0	5.5	V
V _O Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH} High-level output current		-8		-8	mA
I _{OL} Low-level output current		8		8	mA
Δt/Δv Input transition rise or fall rate		20		20	ns/V
T _A Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHCT245		SN74AHCT245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4	4.5		4.4		4.4	V	
	I _{OH} = -8 mA		3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 μA	4.5 V			0.1		0.1	0.1	V	
	I _{OL} = 8 mA				0.36		0.44	0.44		
I _I	\overline{OE} or DIR V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1*	±1	μA	
I _{OZ}	A or B inputs† V _O = V _{CC} or GND	5.5 V			±0.25		±2.5	±2.5	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4		40	40	μA	
ΔI _{CC} ‡	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V			1.35		1.5	1.5	mA	
C _i	\overline{OE} or DIR V _I = V _{CC} or GND	5 V		2.5	10			10	pF	
C _{iO}	A or B inputs V _I = V _{CC} or GND	5 V		4					pF	

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

† For I/O ports, the parameter I_{OZ} includes the input leakage current.

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

SN54AHCT245, SN74AHCT245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHCT245		SN74AHCT245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	$C_L = 15\text{ pF}$	4.5**	7.7**	1**	10**	1	8.5	ns	
t_{PHL}				4.5**	7.7**	1**	10**	1	8.5		
t_{PZH}	\overline{OE}	A or B	$C_L = 15\text{ pF}$	8.9**	13.8**	1**	16**	1	15	ns	
t_{PZL}				8.9**	13.8**	1**	16**	1	15		
t_{PHZ}	\overline{OE}	A or B	$C_L = 15\text{ pF}$	9.2**	14.4**	1**	16.5**	1	15.5	ns	
t_{PLZ}				9.2**	14.4**	1**	16.5**	1	15.5		
t_{PLH}	A or B	B or A	$C_L = 50\text{ pF}$	5.3	8.7	1	11	1	9.5	ns	
t_{PHL}				5.3	8.7	1	11	1	9.5		
t_{PZH}	\overline{OE}	A or B	$C_L = 50\text{ pF}$	9.7	14.8	1	17	1	16	ns	
t_{PZL}				9.7	14.8	1	17	1	16		
t_{PHZ}	\overline{OE}	A or B	$C_L = 50\text{ pF}$	10	15.4	1	17.5	1	16.5	ns	
t_{PLZ}				10	15.4	1	17.5	1	16.5		
$t_{sk(o)}$			$C_L = 50\text{ pF}$			1**			1	ns	

** On products compliant to MIL-PRF-38535, this parameter is not production tested.

*** On products compliant to MIL-PRF-38535, this parameter does not apply.

noise characteristics, $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER	SN74AHCT245			UNIT
	MIN	TYP	MAX	
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}		4		V
$V_{IH(D)}$ High-level dynamic input voltage	2			V
$V_{IL(D)}$ Low-level dynamic input voltage			0.8	V

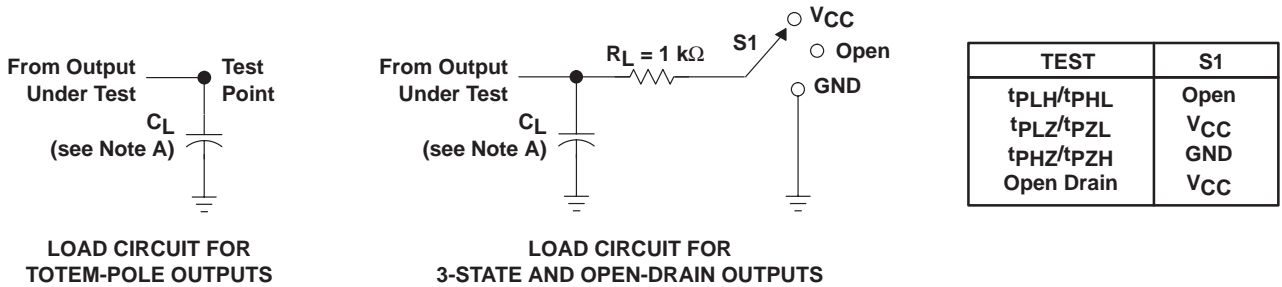
NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1\text{ MHz}$	13	pF

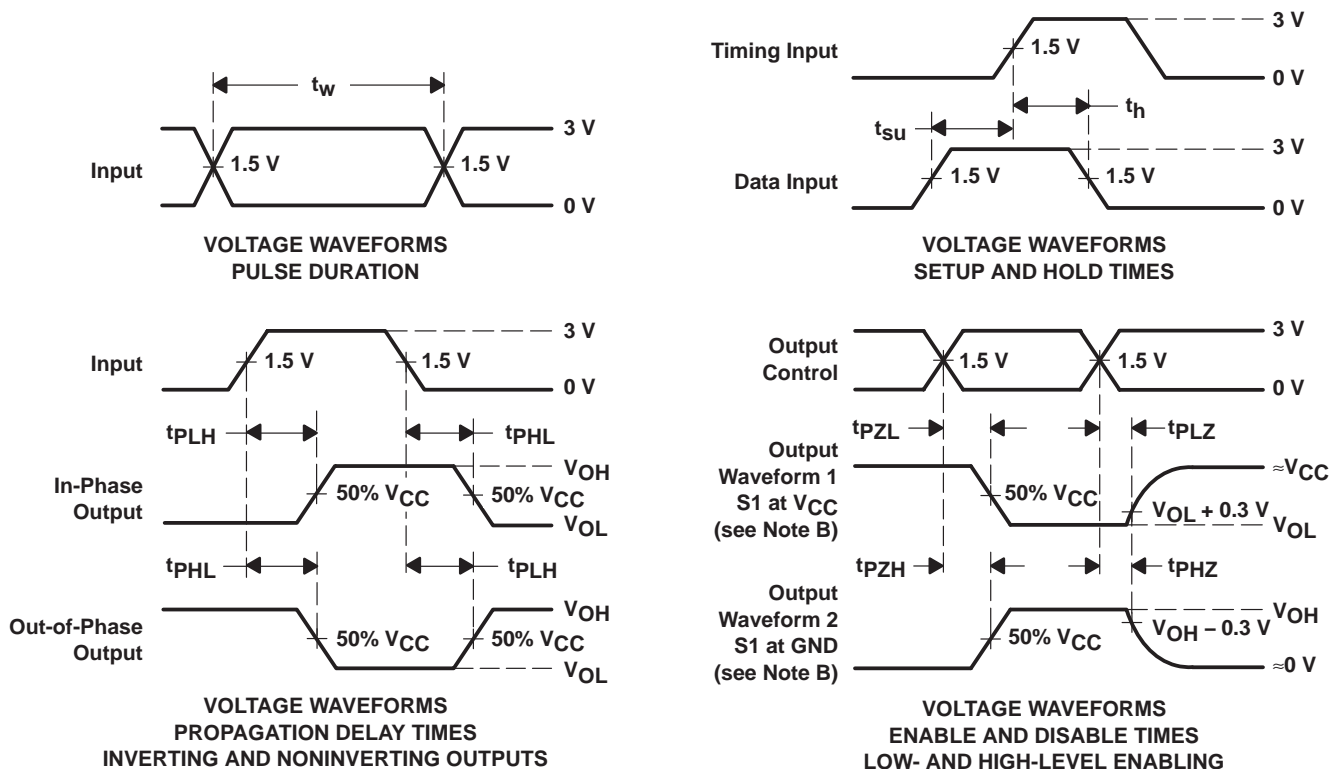


PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns.
 D. The outputs are measured one at a time with one input transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms